## Workshop GDRİ CNRS mecano

# Mechanical Issues for Advanced Electron Devices

**Grenoble, France,**

**June 29-30, 2015**

Chairs :
Olivier Thomas, Mireille Mouis

Website :
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# Program

## Monday, June 29

11:30 12:00 Welcome

12:00 13:30 Lunch

13 :30 13 :45 General Introduction

### Session 1 – Advanced CMOS – Strain Engineering

13:45 14:25 P. Morin (STMicroelectronics) - Strain engineering in advanced CMOS devices (*Invited*)

14:25 14:50 R. Berthelon (STMicroelectronics) - Strain-induced local layout effects in 14FDSOI pMOSFETs with SiGe channel

14:50 15:15 M. Moussavou (IM2NP) - Influence of mechanical strain in Si and Ge p-type double-gate MOSFETs

15:15 15:40 M. Pala (IMEP-LAHC) - Quantum simulation of mobility and current enhancement in sub-14nm strained SiGe fully-depleted pMOSFETs

15:40 16:10 Coffee Break

### Session 2 – Advanced CMOS – Strain characterization

16:10 16:55 S. Escoubas (IM2NP) - Non-destructive strain mapping at the nanoscale by X-ray diffraction (*Invited*)

16:55 17:20 R. Claverie (CEMES) - Process induced strains in FDSOI: a contribution of dark-field electron holography

17:20 17:45 A. Durand (STMicroelectronics) - Composition and strain mapping of a 7-nm-thick condensed Si1-xGex layer by Micro-Raman spectroscopy and Scanning X-Ray Diffraction Microscopy

17:45 18:10 F. Rieutord (CEA INAC) - Contact of surfaces at the nanoscale: the example of wafer direct bonding

18:10 19:30 Poster Session

20:15 Dinner downtown

## Tuesday, June 30

### Session 3 – 2D materials

08:30 09:10 T. Hallam (Trinity College Dublin) - Introducing out-of-plane deformation to layered materials (*Invited*)

09:10 09:35 O. Aydin (IMEP-LHAC) - A study of the residual strain in suspended CVD graphene devices made by a robust fabrication route

09:35 10:00 A. Ghis (CEA LETI) - Implementation and Mechanical Characterization of 2 nm thin Diamond Like Carbon Suspended Membranes

10:00 10:25 W. Venstra (TU Delft) - Strain tuning of $MoS_2$ nanomechanical resonators

10:25 10:55 Coffee Break

### Session 4 – Nanowires

10:55 11:20 A. Heinzig (NamLab TU Dresden) - Mechanical stress as a key enabler for symmetry in reconfigurable silicon nanowire transistors (*Invited*)

11:20 11:45 S. Tardif (CEA) - Strain mapping in Ge microdevices: a combined experimental study

11:45 12:10 G. Signorello (IBM Research Zürich) - Inducing a direct-to-pseudodirect bandgap transition in wurtzite GaAs nanowires with uniaxial stress

12:10 12:30 Closing Remarks

12:30 Lunch

## Attendees

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# Strain engineering in advanced CMOS devices

Pierre Morin
STMicroelectronics

Introducing strain in transistor channels has proven to be a very effective method to boost the transistor performance since the advent of the 90nm complementary metal oxide semiconductor field effect transistor (CMOSFET) technology node. A variety of techniques has been successfully developed to produce devices with strained channel and accelerate the electrical performance while achieving the requirement of yield production and product reliability. To summarize, the introduction of strained in transistor channel has been one of the success story of the CMOSFET industry over the course of the last 15 years.

However, the continuous scaling pace has resulted in substantial reduced volume of stressors with a decrease of the channel strain. To compensate for this loss in mechanical performance, recent devices have embed mechanical stressor exhibiting increased strain up to 2% which might exceed the limit of elasticity. Recent years have also seen the introduction of new device architectures with thin channel such as FinFET or fully depleted silicon on insulator (FD-SOI) which have replaced the traditional planar bulk or partially depleted SOI solutions. Next steps imply further innovations with the use of new channel materials, new architectures and potentially the transition to other switch mechanisms to replace the traditional field effect transistor. These challenges and evolutions questioned the effectiveness of strained silicon techniques for the next technology nodes.

After a brief introduction highlighting the impact of mechanical strain on transport properties and discussing the relevance of strained channel for the performance of the most recent technology nodes, this paper will focus on the mechanical aspects of strained channel engineering. We will review the trends in this domain through the scope of simple elastic consideration highlighting the key material and geometrical parameters of these mechanical systems with a particular focus on the CMOSFET scaling laws. In this frame we think it is time for a transition to different stressor paradigm particularly to handle the scaling constraints. We will also consider some of the material challenges linked to the reduced dimensions of the strained devices. In particular we will put forward the question of the mechanical stability at reduced scale and highlight the challenge linked to the introduction of an increased number of stressor techniques involving mechanisms of plasticity in crystals.

# Strain-induced local layout effects in 14FDSOI pMOSFETs with SiGe channel

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STMicrolectronics and LETI have developed a high-performance and low-power 14nm Fully Depleted Silicon On Insulator FDSOI technology. It features 6nm channel and 20nm buried oxide (BOX) thicknesses. Moreover, for the first time, a dual Si/SiGe channel has been integrated directly on insulator. The strained-SiGe channel of the pMOSFETs is one of the main sources of performance boost with respect to previous nodes. It is realized by a Ge-enrichment process before the Shallow Trench Isolation patterning. Just after its integration, the globally-strained channel yields large and uniform intrinsic strain, compared to process-induced strain techniques (such as recessed SiGe sources/drains or Contact-Etch-Stop-Layers). But both techniques are highly sensible to the device layouts and the process integration. Especially, during the Shallow Trench Isolation (STI) patterning, it is well known that the stress can be altered and thus the device performance changed. As a consequence, the SiGe channel integration raises new challenges in terms of characterization and modelling, especially for the understanding of local layout effects.

In this scope, we fabricated an 8-nm thin compressive SiGe film with 20% of Germanium by epitaxy process on top of Si and we etched the complete stack. The stress profile has been measured using Nano-Beam Electron Diffraction. We evidence a stress relaxation that occurs at the edge of active area. This is due to the presence of a free boundary condition at the edge of the active area. We compare these results with mechanical simulations of compressive SiGe relaxation performed with a finite elements method. A good agreement is obtained with a pure elastic simulation model. At approximately 100nm from the edge, the level of stress still corresponds to the initial stress introduced by Ge integration. At a distance from the edge of approximately 25nm, the level of stress is divided by 2 and finally the stress is null on the side due to the free boundary condition. The resulting stress in the channel is thus strongly anisotropic, depending on the active width and length. Example given, if the pMOS active area is short in one dimension, the remaining stress in the channel is no longer biaxial but becomes uniaxial.

In terms of electrical behaviour, the relaxation that occurs along the active width is beneficial for pMOS, while relaxation along the active length is detrimental to hole mobility. During the patterning of the active area, relaxation occurs at both sides of the rectangular active. There is thus a competition between the performance gain induced by the relaxation along the active width and the loss induced by the relaxation along the other direction. In order to find the best compromise for performance, we developed an analytical model describing the stress relaxation that has been evidenced previously. We use this model in addition with the piezoresistive model in order to evaluate the mobility dependence with active area dimensions. We evidence that an optimum strain profile exists for a given layout (active width and length).

# Influence of mechanical strain in Si and Ge p-type double-gate MOSFETs

Manel Moussavou, Nicolas Cavassilas, and Marc Bescond (IM2NP, CNRS, Aix-Marseille Université)

Strain engineering has been introduced since the 90 nm node as a technological booster to maintain the improvement of performances of Si-CMOS transistors. More recently, Ge channel material has been envisaged as an additional booster of hole's mobility [1,2]. In that context a careful analysis of the influence of channel material, strain and crystallographic orientation is essential to fully assess the potentialities of nano-transistors. The issue is even more complicated when considering p-type devices since both multiband nature of valence-band and hole-phonon scattering may have a substantial impact on current characteristics [3].

In this work we then propose a theoretical study of p-type double-gate Si- and Ge-based MOSFETs for various strain options, channel orientations and channel length's. We use the non-equilibrium Green's function (NEGF) formalism expressed within the six-band k.p Hamiltonian. Acoustic- and optical-phonon scatterings are addressed within the self-consistent Born approximation [4]. Strain is handled through the Bir-Pikus Hamiltonian. Our conclusions show that the best option for long channel transistors (Lg=15 nm) is <110>-compressive Ge-based device due to smaller effective mass and then weaker phonon scattering.

The situation is significantly modified when reducing Lg down to 7 nm. The small effective masses of Ge (from 0.07×m0 to 0.15×m0) are now detrimental and generate a strong tunneling effect through the channel potential barrier. As a consequence, the best performances are obtained in <100>-Si-based devices whose intermediate effective masses ($m^* \approx 0.3 \times m_0$) provide both a good control of the off-regime and a high on-current. In particular optimum current is delivered by the <100>-tensile configuration whose band structures are less sensitive to inter-subband phonon scattering. Note that tensile strain is found to become the worse solution along the <100>-direction in the ballistic regime, demonstrating the importance of phonon scattering in devices of the far end of ITRS.

[1] K. Kuhn, IEEE Trans. Electron Devices, vol. 59, no 7. pp. 1813-1828 (2012).
[2] Rui Zhang et al., IEEE Trans. Electron Devices, vol. 60, no. 3, pp. 927-934 (2013).
[3] N. Cavassilas, F. Michelini, and M. Bescond, J. Appl. Phys., vol. 109, p.073706 (2010).
[4] E. Dib, et al., J. Appl. Phys., vol. 114, p.083705 (2013).

# Quantum simulation of mobility and current enhancement in sub-14nm strained SiGe fully-depleted pMOSFETs

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By means of non-equilibrium-Green's function quantum simulations and bandstructure calculations based on 6 band-k.p Hamiltonians, we study the impact of Ge molar fraction and of the stress orientation on the transport properties of fully-depleted SiGe pMOSFET with different gate lengths. Alloy scattering and acoustic and optical phonons were included within the self-consistent Born approximation and effective mobility extracted in long channel devices according to the method proposed in [1]. Importantly, physical models were calibrated with experimental data on state-of-the-art devices [2]. Our results show that the increase of the Ge molar fraction determines a larger intrinsic biaxial stress of the pseudomorphic SiGe film and that compressive longitudinal stress along the [110] transport direction provides remarkable mobility gains with respect to an unstressed Si device as a result of the strong deformation of valence subbbands induced by the shear strain component.

[1] S.Poli et al., IEEE TED vol. 55, 2968, 2008.
[2] D. De Salvo et al., IEDM 2014, pp. 7.2.1 - 7.2.4, 2014

***Session 2 – Advanced CMOS – Strain characterization***

## Non-destructive strain mapping at the nanoscale by X-ray diffraction

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This study is aimed at the determination of local strain fields in silicon induced by advanced microelectronics process. For that purpose we used X-ray diffraction which is which is very sensitive to local strains (<10-4), and presents the advantage of being non destructive. We show, through two examples, the strain maps determined at the nanoscale thanks to X-ray diffraction coupled with finite elements modelling.

We first studied the strain field in silicon channel induced by a SiN stressor. The deposition of a stressed layer on top of the poly-silicon gate has shown to be both an effective and a cheap way to stress the transistor FET Si channel and enhance electron and hole mobility. In the case of periodic array deposited on silicon, the periodic strain field yields satellites in reciprocal space around unstrained Si Bragg peak, which intensities represent a fingerprint of the strain in the silicon substrate. We explain how we have used the High Resolution XRD technique to refine a mechanical model calculated by finite element modelling, in order to determine the strain field in silicon depending on the nitride properties (young modulus and internal stress) which are strongly dependent on the deposition method.

The second study concerns copper filled through silicon via (TSV) which allow high speed interconnection between 3D integrated circuits. As a result of the confinement of metal filled TSVs and the coefficient of thermal expansion (CTE) mismatch with the surrounding Si matrix, stress is generated both in the TSV and surrounding Si. Local measurements in silicon are performed with the help of micro-Laue diffraction at beamline BM32 from the European Synchrotron Radiation Facility (ESRF). A sub-micrometer polychromatic X-Ray beam is used to extract the local deviatoric strain tensor in silicon over around 30µm probing depth at room temperature. The stress fluctuations in silicon across a 80 µm deep TSVs raw are weak and match the presence of copper-filled TSVs. With the help of the dynamical theory of diffraction a depth discrimination is performed which reveals a stress amplitude modification. Complementary diffraction experiments were performed using a nano-focused X-ray monochromatic beam at the ID01 beamline of the ESRF. An advanced technique which consists in a two-dimensional (2D) quicK continuous Mapping (K-Map) of the sample at a given reciprocal space position is used. This technique allows for imaging one component of the strain tensor over a 100 µm x 100 µm area with 500 nm step size. We compare thermally-induced strains in silicon around copper filled TSVs, at room temperature and around 400 °C (which corresponds to the TSVs annealing temperature) with finite elements modelling.

# Process induced strains in FDSOI: a contribution of dark-field electron holography

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Strain is an integral feature of FDSOI devices, boosting carrier mobility. However, the strain intentionally introduced by specific techniques, such as the deposition of intrinsically stressed liners or the hetero-epitaxy of SiGe alloys, is often different from expectation because most of the processes used to fabricate the devices impact this strain.

In this contribution, we will describe the dark field electron holography (DFEH) technique able to map strain in two dimensions with nanometer resolution and high precision and the I2TEM microscope specifically designed for running such experiments. We will focus on two examples of processes which dramatically affect strain during the fabrication of CMOS. First, we will show the interplay between composition and strain which takes place during the conversion of the Si-top into a SiGe layer by the Ge condensation technique. We evidence the two different mechanisms driving the redistribution of Ge atoms during this process. The second example concerns the co-integration of Si and SiGe top-layers as required for the fabrication of n and p-MOS. We will follow the evolution of strain in such layers along their fabrication route, from the selective formation of the SiGe layer, to the opening of the trench and the fabrication of the STI, including some post annealing. This analysis will combine results obtained by DFEH with those obtained by the Nano Beam Electron Diffraction (NBED) technique. The comparison with FEM simulations of stress/strain transfer in such structures allows identifying the origin of the resulting strain and sometimes evidences the role of “ingredients” which were not initially considered as important.

# Composition and strain mapping of a 7-nm-thick condensed Si1-xGex layer by Micro-Raman spectroscopy and Scanning X-Ray Diffraction Microscopy

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Among the wide range of materials used with the aim of improving transistor performance the silicon-germanium alloy (SiGe) is being used as a replacement for Si channels since it achieves higher mobility and improves the threshold voltage. Monitoring the compositional and strain homogeneity of this layer which is at the heart of the technology is therefore of high importance. µ-Raman spectroscopy and HRXRD are very promising techniques for in line characterization of strain and Ge content of SiGe epilayer, since they are non-destructive and have a high sensitivity to strain.

In a previous work [1], using µ-Raman, we mapped a structure of 50*100µm composed of a Fully Depleted – Silicon On Insulator (FD-SOI) transformed via the condensation process into a 7-nm-thick strained SiGe layer. In that study, we developed an original approach using both Raman shift and intensity ratio in order to evaluate independently both the Ge composition and the strain state. This analysis highlighted that the strain and Ge content of SiGe epilayer obtained by condensation could be inhomogeneous at the micron scale, with likely critical consequence on technological process implementation.

In order to confirm this important result, we also performed high resolution X-ray diffraction with the same sub-micrometers probe size confers by µ-Raman. For that purpose, we used the fast K-Map method newly developed on ID01 synchrotron beam-line at ESRF [2]. This method allows for fast reciprocal space map measurements with a 200nm spatial resolution on areas of few tens of $\mu ms^2$ in reasonable total time of acquisition. Finally the spatial strain or Ge content mappings can then be directly compared to the Raman measurements.

In spite of the high brilliance of the x-ray beam, in such very thin layers obtained by condensation, the intensity of the diffracting peak is quite weak and we have limited our collection to an area of 10*15µm whereas 50µm*50µm was studied using µ-Raman. We were able to distinguish SiGe from Si peak and clearly appreciate both SiGe peak position shift and intensity variations as expected. We established a partial correlation with the results obtained by µ-Raman and confirmed the inhomogeneity of the SiGe layer obtained by condensation.

[1] A. Durand, D. Rouchon, D. Le-Cunff, and P. Gergaud, “Micro-Raman spectroscopy as a complementary technique to high resolution X-ray diffraction for the characterization of Si 1-x Ge x thin layers,” Phys. Status Solidi, vol. 6, p. n/a–n/a, Feb. 2015.
[2] M. H. Zoellner, M. Richard, G. A. Chahine, P. Zaumseil, C. Reich, G. Capellini, F. Montalenti, A. Marzegalli, Y. Xie, T. U. Schu, P. Storck, and T. Schroeder, “Imaging Structure and Composition Homogeneity of 300 mm SiGe Virtual Substrates for Advanced CMOS Applications by Scanning X ray Di ff raction Microscopy,” 2015.

We acknowledge the European Synchrotron Radiation Facility for provision of synchrotron radiation facilities and especially the ID01 beamline staff for support during the K-map experiments. The ESRF beamtime have been funded by the ANR- IRT program.

## Contact of surfaces at the nanoscale: the example of wafer direct bonding

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The interface between two contacting solids can be studied using X-ray scattering techniques. This allows a rather detailed description of the mechanisms at play during direct bonding of semiconductor wafers. We can evidence the presence of a nanogap at the interface between solids using these techniques, whose main features can be measured. We could demonstrate that adhesion between silicon wafers can be described using models between contacting rough surface solids, interacting via compression of the highest asperities. We will concentrate on the hydrophobic bonding case, showing that varying the lateral wavelength of the asperities allows a collapse transition to be evidenced, with interesting practical consequences.

***Session 3 – 2D Materials***

## Introducing out-of-plane deformation to layered materials

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Despite naturally occurring roughness in graphene and unintentionally induced wrinkles during its processing, 2D layers have always been treated as flat sheets. Few studies have been undertaken to create 3D structures from 2D layers. In this work we have used elastomeric stamps with periodically varying adhesive properties to introduce structure and print folded graphene films. In addition to the theoretical and scientific interest, the ability to controllably form folds in monolayer materials has significant technological applications, in particular in electronics and optics.

# A study of the residual strain in suspended CVD graphene devices made by a robust fabrication route

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High stiffness and low mass make suspended graphene an ideal candidate for NEMS while RF applications benefit from its high electrical mobility. Regardless if the devices are supported on SiO2 or if they are suspended, it is crucial to have a large-scale fabrication route. We developed a robust and scalable fabrication route for suspended devices from CVD graphene towards industrial applications. Indeed, we repeatedly achieved fully self-supported graphene beams in all of the 14 devices on each sample but one or two by taking particular care of the etching mask/graphene interface. In addition, we saw that it is possible to suspend more complicated geometries such as Hall bars which are intended for more elaborate electrical measurements including the extraction of Hall mobility and elimination of contact resistance in suspended graphene structures.

In addition to a robust fabrication route, we studied strain-induced effects during fabrication. Firstly, by Raman measurements, we investigated residual compressive strain which is a combined result of the high thermal budget of the CVD process as well as the negative thermal expansion coefficient of graphene. While residual compression is partially relaxed into folds, Raman spectroscopy showed that the compression is, in fact, not fully relaxed even at the final step of fabrication. Furthermore, we looked into fold formation in graphene and have seen that it was possible to promote or impede periodic fold formation perpendicular to the beam length by manipulating fabrication parameters. Once formed, such folds survived heat treatments as well as suspending. Folds, especially sharp ones are predicted to influence local electronic properties as well as chemical reactivity. Therefore, it is imperative to have control over their formation.

# Implementation and Mechanical Characterization of 2 nm thin Diamond Like Carbon Suspended Membranes

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Ultrathin Diamond Like Carbon (DLC) layers with thickness down to 2 nm have been integrated into suspended membranes enabling their mechanical properties to be characterized.

The goal of this study is the integration of a membrane with micrometric suspended area into operational MEMS. The early structure for feasibility study of a device is made of a membrane suspended above a micrometer sized cavity. Deflection is electrostatically induced by applying an electric potential between the membrane and the floor of the cavity. The thickness of the membrane determines at first order the amplitude of the deflection.
Experimental measurements are presented and results obtained discussed. The experimental bending rigidity value is extracted and is shown to be a key parameter for modelling membrane's behavior in any other mechanical embodiment.

DLC is identified as a suitable material for free standing over a micrometer large area, even when only a few nanometer thick, and a promising candidate for MEMS integration.

## Strain tuning of MoS2 nanomechanical resonators

W. Venstra
TU Delft, The Netherlands

Nanomechanical resonators made from suspended 2-dimensional materials have interesting mechanical, optical and electronic properties. Interferometry enables the characterization of their motion with frequency, time and spatial resolution. A review will be given on how these measurements contribute to the understanding of the membrane to plate transition, frequency fluctuations, and geometrical imperfections, and our initial results of their strain-dependent dynamic properties will be discussed.

References:

1. E. Kramer, J. van Dorp, R. van Leeuwen, & W.J. Venstra. Strain-dependent damping in nanomechanical resonators from

thin MoS2 crystals (in preparation)

2. R. van Leeuwen, Castellanos-Gomez, G.A. Steele, H.S.J. van der Zant, & W.J. Venstra. Time-domain response of atomically thin MoS2 nanomechanical resonators. Appl Phys Lett, 105 (2014) 041911.

3. A. Castellanos-Gomez, R. van Leeuwen, M. Buscema, H.S.J. van der Zant, G.A. Steele, & W.J. Venstra. Single-layer MoS2 mechanical resonators. Adv Mater 25 (2013) 46.

***Session 4 – Nanowires***

## Mechanical stress as a key enabler for symmetry in reconfigurable silicon nanowire transistors.

André Heinzig (a), Jens Trommer (b), Tim Baldauf (a), Thomas Mikolajick (a, b), Walter M. Weber (a, b)

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The implementation of devices with multiple functionalities holds the promise of advancing electronics beyond the expected end of classical transistor scaling. Recently, several approaches have been demonstrated which show increased functionality by combining the function of an n-type and p-type transistor in one single device. Whether these so-called polarity controllable or reconfigurable devices will have an impact on future electronics depends on the ability to realize CMOS circuits, which is the dominating circuit scheme since the late 1970's.

The fundamental requirement to enable CMOS operation is that the connected complementary pairs of n- and p-type transistors provide absolute equal on-currents, comparable turn-on threshold voltages, and switching slopes. In conventional static devices this electrical symmetry can be realized by independent p- and n-type transistor optimization, for example by doubling p-type transistor width. In multifunctional and reconfigurable devices this methodology is not applicable, since the same device operates as both p- and n-type transistor.

In this talk, it will be shown that applying mechanical stress on nanoscaled transistors can solve the dilemma of adjusting the dependent electron (n-type) to hole (p-type) conduction for multifunctional devices. The key enabler to change the p- and n-type currents is the selective tunability of the tunneling transmission of charge carriers. This has been rendered by the application of radially compressive strain to the two independently gated Schottky junctions of our reconfigurable silicon nanowire transistor (RFET). It has been fabricated by self-limiting oxidation of a silicon nanowire in <110> crystal direction and subsequent silizidation. A highly stressed NiSi2 – Si –NiSi2 nanowire heterostructure with a diameter of 12 nm within a surrounding oxide shell was realized by this procedure. The strained RFET exhibits ideal symmetry as will be shown by the p- and n-configured transfer characteristics.
A demonstrative example of the circuit maturity will be given by the integration of two identical RFETs in series into a single nanowire. Different program voltages are used to combine a complementary pair of p-configured and n-configured RFET. The single nanowire circuit shows ideal complementary function in terms of switching point and cross current restriction, which validates the CMOS functionality of the concept.

Furthermore, the inverter exhibits the same characteristic after switching both transistors to their inverse configuration, demonstrating the full CMOS reconfigurability on the circuit level. Additionally, some examples will illustrate that the implementation of such transistors can lead to a reduction of transistor count or can increase the system functionality as an approach for realizing electronics beyond the limits of classical transistor scaling.

# Strain mapping in Ge microdevices: a combined experimental study

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In semiconductors, charge carrier mobilities and bandgap energies can be controlled by the strain state in the device. The mechanical reliability of the device is also tightly bound to the local strain distribution. It is therefore highly desirable to be able to measure and map the strain in-situ in actual microdevices.

The strain (and stress) state at any given location in a material is described by a 3x3 tensor, i.e. 9 parameters. Additionally, strain can vary locally quite rapidly, at scales smaller than the device considered and the actual amplitude of the maximum displacement may be a few percent at most. Finally, small and sensitive devices may also be affected by the measurement probe, and even destroyed in the worst case. As a result, strain mapping requires multiple, local, precise and fast measurements. An experimental technique that can fulfill all these requirements is still a materials scientist's dream and in the real world, one has to compose with existing non-destructive solutions such as Raman spectroscopy and X-ray diffraction.

Raman spectroscopy has the advantage of being well spatially resolved (even the depth sensitivity can easily be tuned), fast and readily available in the lab. The Raman frequency shift yields an estimation of the strain in a specific crystallographic orientation. Monochromatic synchrotron X-ray microdiffraction can provide a direct measurement of the atomic planes spacing with sub-micron resolution, but several orientations must be measured successively (each with a different beam footprint) in order to resolve the full strain tensor. White beam Laue microdiffraction can overcome this limitation by measuring simultaneously tens of different orientations, at the cost of losing the absolute value of the atomic plane spacing as only the non-homothetic symmetry changes can be observed.
In this presentation, we show how we have combined these different techniques to compensate their respective shortcomings. We could then get a complete picture of the strain in state-of-the-art suspended germanium microdevices (such as microbridges and nanowires) under a wide range of tensile stress. We also discuss how Laue microdiffraction can be used to get the full strain tensor, either numerically with the assumption of stress-free surfaces or experimentally by using the “rainbow” technique.

# Inducing a direct-to-pseudodirect bandgap transition in wurtzite GaAs nanowires with uniaxial stress

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Semiconductors are typically classified either as direct-bandgap materials, known for their efficient light-emission properties, or as indirect-bandgap materials, often used in light-harvesting applications and photo-detectors. The less known pseudodirect bandgap configuration can be found in Wurtzite semiconductors: in this case, electron and hole wavefunctions overlap strongly but optical transitions between these states are impaired by symmetry. Switching a material between bandgap configurations would enable novel photonic applications but large anisotropic strain is needed to induce such band structure transitions.

Here we show that Wurtzite GaAs nanowires can be switched reversibly between direct and pseudodirect bandgap configuration under the influence of a small uniaxial stress. When tensile stress is applied, the direct configuration can be obtained and the nanowires emit light efficiently; upon compression, the pseudodirect configuration is achieved and light emission can be reduced by more than three orders of magnitude. We demonstrate a remarkable energy shift of the PL due to transitions between the bright conduction band state and the heavy hole band (345meV) or the light hole band (257meV), by varying the strain over a range of ±2%.

Using Raman scattering spectra as a relative strain gauge and fitting the optical transition energies to a k•p model, we determine all bandstructure parameters of the Wurtzite GaAs nanowire in unstrained conditions, i.e. the bandgap (1.41eV±8meV), the crystal field (197meV±50meV) and spin-orbit splitting (293meV±129meV) and, most importantly, the splitting between the bright and the dark conduction bands (33meV±47meV). These results provide, for the first time, a conclusive picture of the energy and symmetry of the valence and conduction band states in GaAs Wurtzite, and constitute a solid foundation to the understanding of strain effects on the optical and electronic properties of III-V nanowires.

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## Large Frequency and Quality Factor Enhancement in TaSe2 Nanomechanical Resonators by Laser-Oxidation

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Van der Waals crystals have extraordinary electronic and mechanical attributes (high Young's modulus, elasticity and breaking strength)1 and low mass, and thus these materials could be suitable for making ultimate nano-electromechanical systems. However, such devices typically suffer from low quality factors (100-2500)2.
In this work, we demonstrate the enhancement of the quality factor and frequency on ultrathin TaSe2 based mechanical resonators by a laser irradiation process. TaSe2 drumhead resonators of different thicknesses are fabricated, and their frequency spectra are measured with an interferometry technique3. When the drums are irradiated with a high power laser, they undertake an oxidation process resulting in a dramatic increase of their stress (8 times increase). This large stress results in drastic increases of Q and f for the ultrathin drums.

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# GaN Nanowire Based Flexible Sensor for Structural Health Monitoring Applications

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Gallium nitride (GaN) nanowires are used to build up capacitive flexible piezoelectric sensors dedicated to structural health monitoring. These cone-shaped nanowires with a hexagonal cross section are grown on sapphire substrate by Metal Organic Vapor Phase Epitaxy (MOVPE); their length can vary from few microns up to hundreds of microns, while the conicity angle evolves in the 0.1°-1.2° range. Nanowires are assembled into a capacitive structure on a flexible substrate using the Langmuir-Blodgett method. As the nanowire geometry (i.e. length and conicity) depends on the growth conditions, the response of the device with embedded nanowires may vary accordingly. In this work, we investigate in depth the impact of these two parameters on the potential generated by single hexagonal nanowires embedded in parylene. Based on such studies, our aim is to figure out the best-suited geometry for the targeted application.

Finite element modelling (FEM) software was used to build up the sought geometry and simulate the electrical behavior of the piezoelectric nanowire when subjected to bending. The structure was obtained in the software from a hexagon section extruded along a certain axis with a fully parametrized extrusion ratio properly calculated in order to achieve realistic conical shapes. Geometry and constraints were simulated so as to be able to perform parametric studies on the two main parameters: length and conicity angle.
The nanowire piezo response in terms of potential (V) and piezo polarization, which is the charges generated by unit area, were simulated. Studies have been conducted taking into account both surface and volume effects, since the physical phenomena behind potential generation are surface related. Thus, the behavior of nanowires with different length or conicity angles but with identical surfaces or volumes were compared with a view to quantifying and evaluating their influence on the single nanowire response, hence on the overall flexible sensor response.

Relying on these results, we were able to figure out an appropriate nanowire geometry for integration within the sensor. The fabrication methods will be subsequently adapted so as to obtain suitable shapes. Depending on the targeted properties of the sensors, we would either go for short nanowires with high conicity or ultra long nanowires with moderate conicity angles.

# Packaging Induced Stress effects in advanced semiconductor products: implementation of sense structures on 40nm CMOS technology node and prediction of device shifts.

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While semiconductor technology advances, packaging needs to be considered from both fracture mechanics and circuit performances points of view. Within this framework, this work aims at implementing sensors in order to determine the electrical responses of device due to packaging stress. To do so, MOS rosette sensors and bandgap structure, embedded into a CMOS40nm test chip, are investigated.

Calibration is first made thanks to four point bending machine, resulting in the extraction of the piezoresistive coefficients of 4n&4p MOS rosette sensors, and the determination of the sensitivity of bandgap structure with respect to stress. In addition, 3D finite element simulations on typical configurations of a moulded BGA package are performed with the Ansys software. More precisely, the influence of the die size on device performance is identified.

Packaging stress, related to the moulding compound reflow step is simulated by a cooling from 225°C down to 25°C. CTE mismatch between materials generates high biaxial compressive stresses in the single crystalline silicon (i.e. the active part) of the die (sxx=syy=-215MPa for large die, sxx=syy=-160MPa for small die) over a large area at the centre of the dies.
Then, introducing the piezoresistive coefficients aforementioned, the mobility change of the functional MOS is evaluated, showing significant mobility changes in distinct regions of the die: up to -11% diminution was found on nMOS, while pMOS are boosted up to +5%. Furthermore, intra die mobility variation is evaluated around 2%. On the other hand, the larger the die is, the higher the variations are.
Beyond effects of stress on functional MOS and to state on the stress influence at circuit scale, a bandgap structure is also analysed.
Bandgap is a reference and complex structure composed of many components namely resistances, CMOS and BiCMOS, having conduction channels oriented in different silicon crystallographic directions. Dedicated simulation strategy is then proposed to make the bridge from the bandgap coefficients previously calibrated to the stress components. Package simulation results show variations of the output voltage around -0.36% at the central region of the large die and -0.24% for the small one.

These studies demonstrated that effects of packaging steps at the transistor and circuit scales cannot be neglected anymore.
In addition, the influence of the die size on MOS mobility and bandgap output voltage was highlighted. This work allows further optimization and improved design for products performance management.

# 2D TCAD strain simulations from fully depleted to nanowire transistors: Efficiency of mechanical stressors.

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Stress engineering is one of the most promising mobility boosters for advanced CMOS technology nodes. Technology Computer Aided Design (TCAD) simulations that account for mechanical strain are increasingly used to develop and optimize CMOS process and to provide guidelines for strain engineering. Here, TCAD simulations of fully-depleted silicon on insulator (FDSOI) and nanowire (NW) transistors were performed with the SProcess tool [1] for a realistic process flow [2-3-4]. Simulations were done under the assumption of plane strain and purely elastic materials. The mechanisms for stress generation included lattice mismatch between silicon and SiGe layers,[5] as well as thermal mismatch [6] and intrinsic stress [7], which depend on deposition techniques. For gate stack materials, the residual stress values used as simulation inputs were taken from experiment.

Two kinds of wide FDSOI structures were studied. The “regular device” is assumed to be repeated with the standard repetition pitch and is thus bounded by adjacent devices while the “isolated device” is delimited by STI (shallow trench isolation). With this study, we analyzed the impact of gate length, raised SiGe source/drain (S/D) and STI in terms of stress level enhancement in the channel of p-type FDSOI transistors for the 14-nm technology node. Germanium content was set to 23% in the channel (~1.6GPa initial biaxial compressive stress). We particularly focused on evaluating two advanced straining techniques: the “gate last” option [2], and self-aligned in-plane stressors where Ge content is increased below S/D contacts to further compress the channel. [4] We found that TCAD mechanical simulations were in close agreement with strain maps obtained by precession electron diffraction (PED) as shown by a comparison performed before dummy gate removal during gate last processing.

In the case of narrow FDSOI devices (NW transistors), we started by simulating n-type long devices on strained SOI (sSOI), where we studied how strain in device cross section was influenced by gate stack and especially by the gate patterning of a TiN metal gate. As expected, the initially biaxial stress in sSOI (1.4GPa tensile stress) was turned into a uniaxial stress after active region patterning. Finally, TCAD simulation results across nanowire channel were correctly matched with experimental nano-beam electron diffraction (NBED) data [8].

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## Bending piezoelectric nanowires: application to force-displacement sensors based on individually interconnected vertical piezo-semi-conductive nanowires.

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One-dimensional nanostructures exhibit a large range of potential applications in nano-electronic devices. In particular, vertical piezo-semi-conductive nanowires (NWs), such as Zinc Oxide (ZnO) or Gallium Nitride (GaN) NWs, have been considered and studied for high sensitivity sensor applications.
In this work we analyze a force-displacement sensor based on an individually contacted vertical piezo-semi-conductive NW matrix. The purpose of the present study is, on one hand, to investigate the pixel piezoelectric response. On the other hand to touch on device's feasibility.

Two key points are mainly addressed: (i) the analysis of a single pixel, i.e. a single interconnected NW, by Finite Element Method (FEM) simulations taking into account the surrounding environment of the NW within one pixel (seed-layer, a part of silicon substrate, two electrodes). It was found that the bottom region of the NW, the so-called piezopotential inversion region, hosts the highest piezopotential values in our configuration. This is where the electrodes should be placed. We show that piezopotential spreads from this region to the seed-layer, and that thinner seed-layers are to be preferred. Tolerance regarding process variability directly correlated to device's fabrication was also analyzed. (ii) The progress achieved for device fabrication. We mainly report the influence of clean-room processed seed-layers on ZnO NWs features obtained by hydrothermal growth.
Our model predictions and NW growth experiences provide guidance for device design and fabrication.

# Study of the effects of the heterogeneities on the electro-mechanical responses of a complex system

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With the development of the "Internet of Things" in the recent years, the idea of integrating electronic components in textiles is becoming more and more common. Primo1D, a young and innovative French Start-up has taken up the challenge of creating "intelligent" textile yarns – the E-Thread® – by directly merging micro-electronic components with textile yarns. Like every other innovation, this one has to address scientific and technical challenges, one of those being the understanding of the interaction between the different elements (the conductive wires, the chip, the textile threads …) while being under stress. To resolve this, a Ph.D. was started in partnership with the Center for Material Sciences of Mines ParisTech in Évry, France and the CEA/LETI in Grenoble, France. The purpose of this poster is to present how this Ph.D. will try to understand and resolve this challenge by way of physical and mechanical finite element simulations with hierarchical multi-scale models and comparisons with experimental results. In particular, this poster will explain how we will study the effects of the heterogeneities on the system electro-mechanical responses.

## Piezoresistive properties of NMOS and PMOS Omega-Gate SOI Nanowire transistors.

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We present an experimental study of strain effects on silicon NMOS and PMOS TriGate (TG) nanowire (NW) MOSFETs featuring state-of-the-art technology with channel cross-section down to 10nm×10nm and channel length down to 20nm. The piezoresistive coefficients have been measured for various technological splits and from the low to high stress regime (stress in the channel above 1GPa). Scaling effects of channel width WNW, channel height HNW and gate length are presented experimentally and discussed theoretically. The effect of additional stressors (i.e. SiGe S/D, tensile or compressive CESL) has also been investigated. We have shown that the conventional definition of the piezoresistive tensor does not work with aggressive channel width scaling. A specific strain effect was highlighted for TG NW transistors below a critical width of 100nm, and for channel height of 11nm. Finally, we have drawn an empirical model based on simple assumptions and density carrier simulations. This model fits, with comfortable accuracy, the behavior observed with channel width shrinking in term of both mobility and piezoresistive coefficients variation.

# High Energy Pencil Beam X-Ray Diffraction : A New Approach to Probe Strain at the Nanoscale

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A single scan approach (i.e. compatible with various in-situ conditions) is proposed to evaluate chemical and structural gradients in polycrystalline thin film with deca-nanometric resolution [1,2]. Samples are measured in cross-section in transmission geometry using a X-ray nano-pencil beam. Powder diffraction methods are usable thanks to this strong asymmetric beam shape (i.e. large number of diffracting grains).
2D diffraction pattern composed of numerous Debye rings is used to determine micro-structural information. In depth strain/stress profile is deduced using sin2 psi or crystallite group method, texture using azimuthal ring intensity and grain size information using various line profile analysis). The efficiency of the approach will be illustrated with sereval examples coming from microelectronic and nanotechnology topics (Cu direct bonding, PZT or ferritic thin films). Finally, in-depth resolution, technique throughput (sample preparation, alignments) and accuracy are discussed.

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## Investigating temperature-dependent die curvature during silicon interposer integration.

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In response to standard packaging technologies, 2.5D silicon interposer technology is constantly catching attention with the window of opportunities it provides in the field of high wiring density, system partitioning, cost efficiency, low power and stress relief in fragile low-k dice. However, because of interposer's typical large size (> 200 mm²) and die thinning processes involved during its integration, thermo-mechanical reliability constitutes one of the most challenging issues concerning volume manufacturing. Mechanical stress which originates from the mismatch of coefficient of thermal expansion (CTE) between deposited materials can alter die stacking steps due to the important curvature generated at die-level.
Several characterization techniques are used and compared in this work in order to investigate curvature phenomena. As previously discussed in studies related to the deformation of thin-film/substrate systems, non-uniform curvatures are found for several specimens and prevent the use of Stoney's law to predict thin-films stress based on a uniform curvature assumption. Following the evaluation of single layers contribution to overall curvature, a finite element model is proposed to describe nonlinear behaviors as measured experimentally.

The aim of this study is to develop a viable strategy of curvature compensation by depositing on the backside of the die one or several dielectric layers whose optimal residual stress is calculated and controlled.

# Notes

## Notes