Device Related Characterization Techniques for Si/SiGe Heterostructures

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Outline

- Strained Silicon MOSFETs
- Thin Strain Relaxed Buffer (SRB) MOSFETs
- Characterization
- Summary

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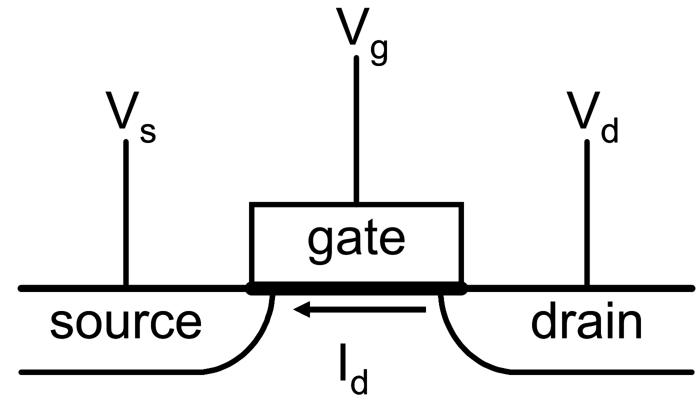
Strained Si: Virtual Substrate

Si Technology

- Cheap, well-developed
- Device scaling → higher performance devices
- Increasing fabrication costs
- Physical limits
- Alternative material systems



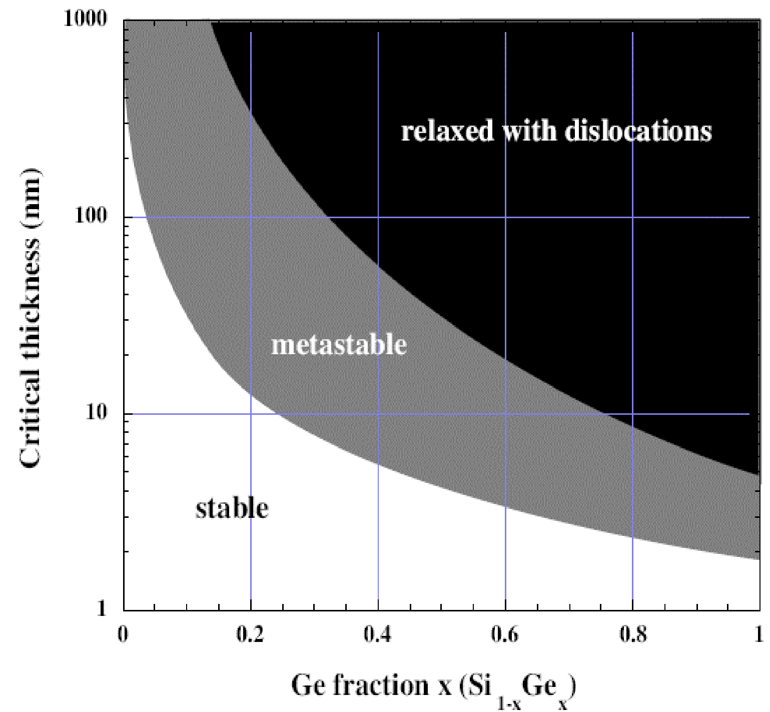
Strained Si/SiGe Technology

- Lattice mismatch →strained Si → higher mobility
- Higher speed/lower power devices
- Less aggressive scaling
- Compatible with conventional Si
- Cost

Challenges of strained Si/SiGe MOS technology

Critical thickness and strain relaxation

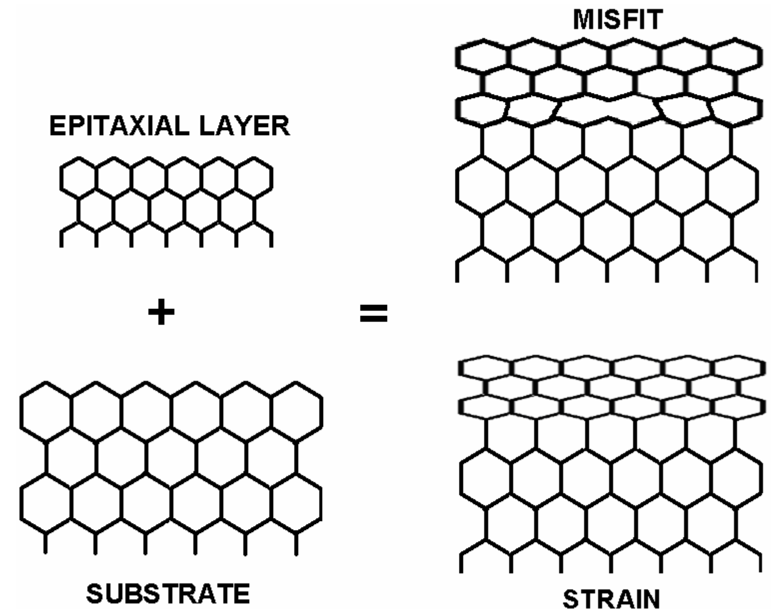
- **Increased lattice mismatch**
  - increased strain in Si
  - increased mobility
- **But increased lattice mismatch**
  - reduced critical thickness



Challenges of strained Si/SiGe MOS technology

Critical thickness and strain relaxation

- **Strain relaxation causes**
  - Loss of enhanced mobility
  - Generation of defects
  - Leakage paths
  - Scattering centres



Challenges of strained Si/SiGe MOS technology

- **Strain relaxation avoided by:**

Thin strained layers

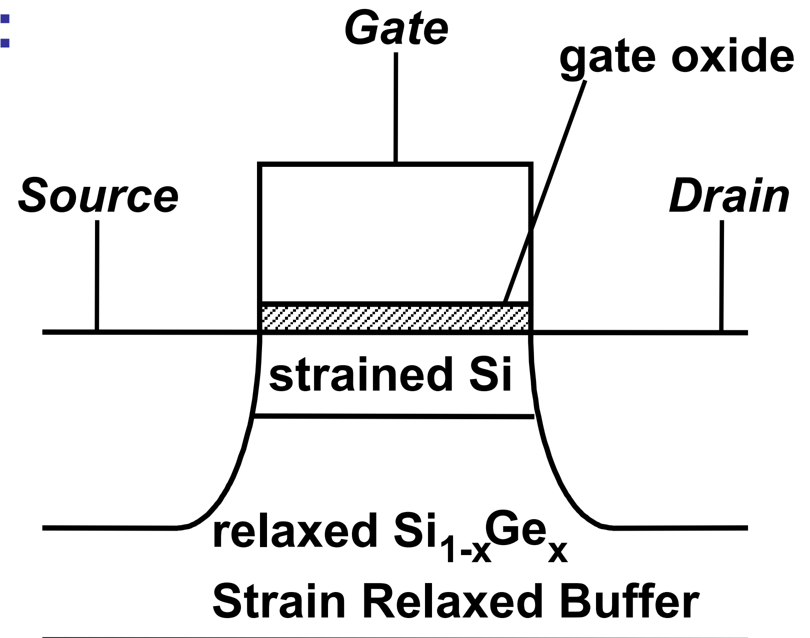
- channel thickness, oxide quality

Reduced lattice mismatch

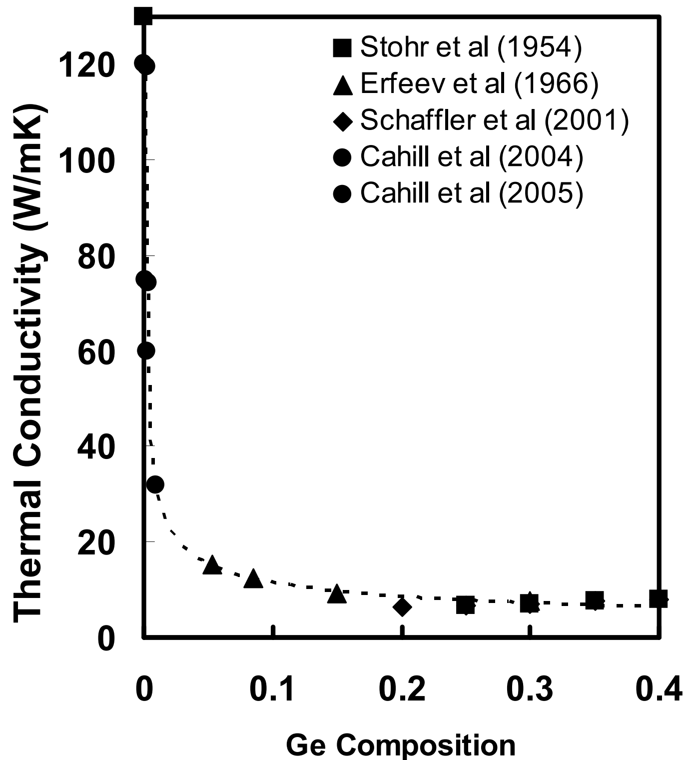
- performance gains

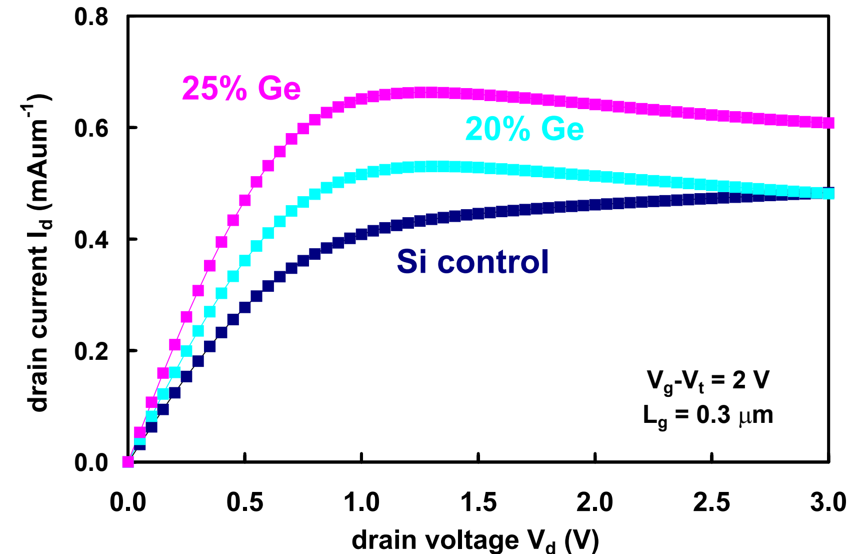
Low thermal exposure

- processing, performance



Maximising performance in strained Si MOSFETs





- Thermal conductivity SiGe << bulk Si
- Poor power dissipation in strained Si/SiGe devices
  - => increased device self-heating
  - => compromised performance gains

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- Thin Strain Relaxed Buffer (SRB) MOSFETs
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Thin SRB MOSFETs

Advantages

- Minimises self-heating
  - Improved performance, particularly for analogue applications
- Economical
  - Thinner layers require less growth time
  - Reduced material consumption
- Virtual substrate designs
  - Potential to introduce large amounts of strain
  - Enhancements at conservative geometries
  - Design flexibility (single channel, dual channel, resonant tunnelling diodes, HBTs …)

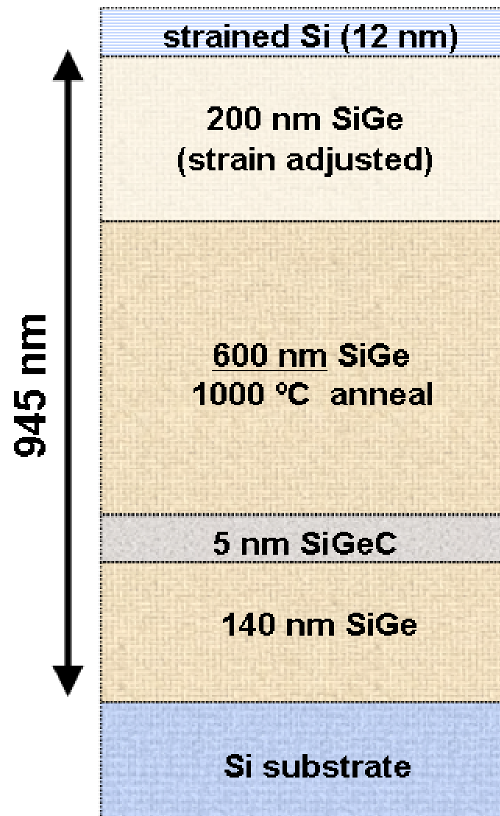
Thin SRB MOSFETs

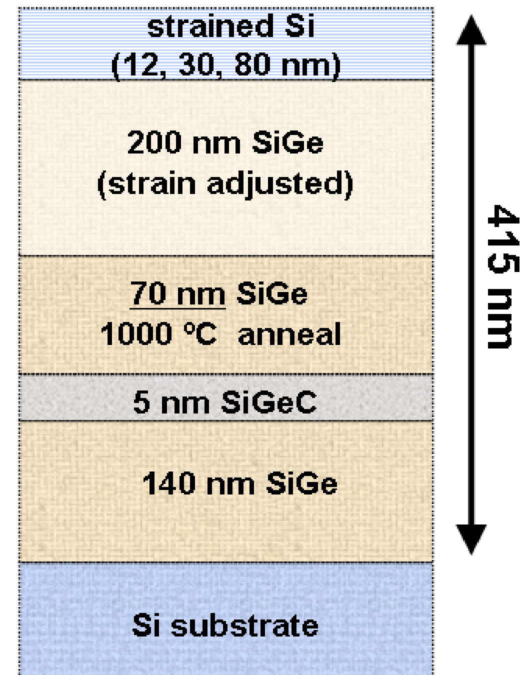
Challenges

- Strain generation
  - can full relaxation be achieved in a thin SRB?
- Strain ‘robustness’
  - is thermal stability affected by incomplete SRB relaxation?
  - is the critical thickness affected?
- Material quality
  - will roughness increase from the close proximity of dislocations?
  - will surface defect density be sufficiently low?
- Device performance
  - will the above factors enable performance enhancements?

Material

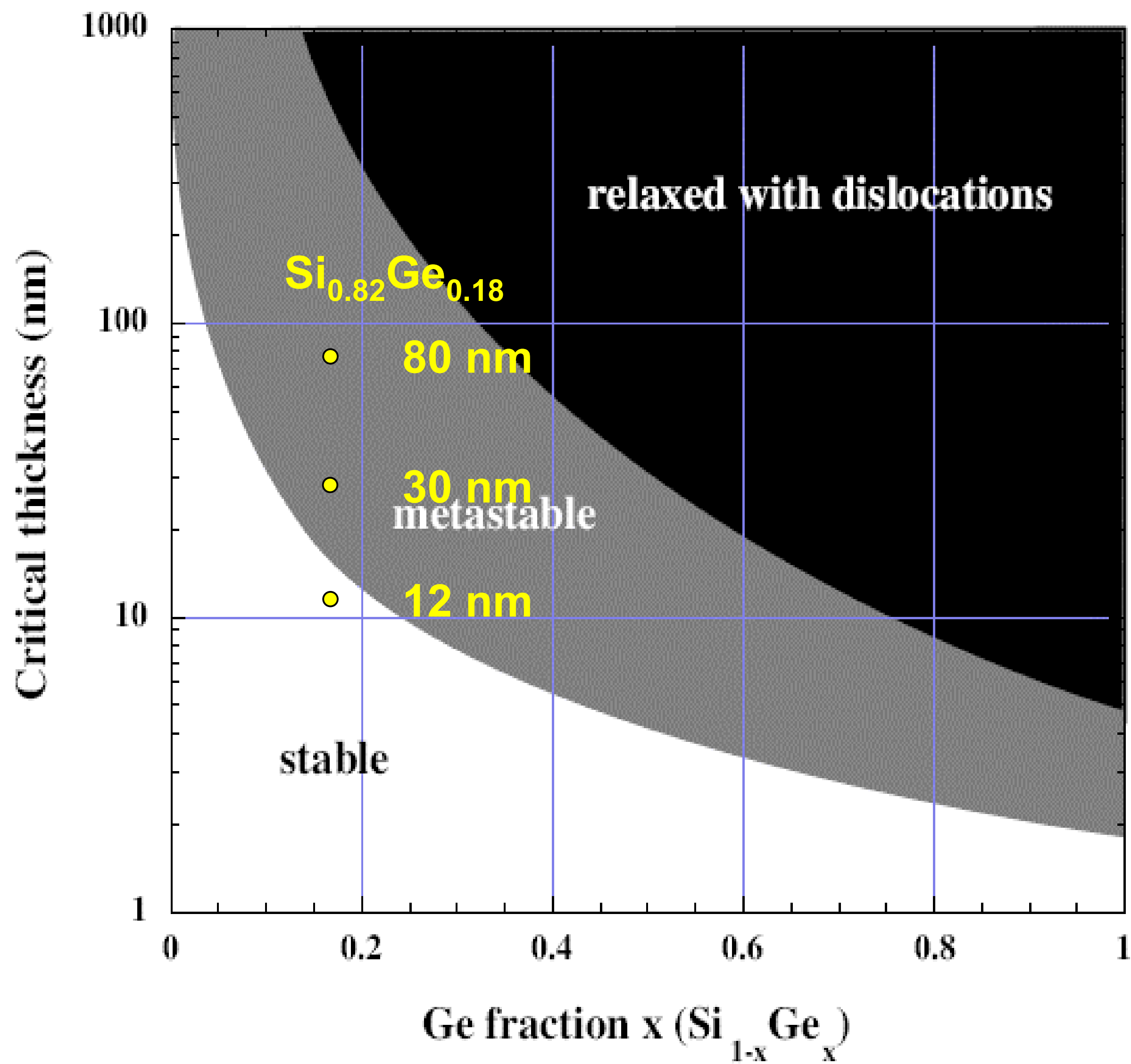
- ASM Epsilon 200mm
- SRB Growth at 600C
- C incorporation
  → relaxation through dislocation formation
- $Si_{0.78}Ge_{0.22}$ with 75% relaxation
- Further relaxation after 30 s anneal @1000C
- $Si_{0.82}Ge_{0.18}$ strain adjustment layer





thick substrate

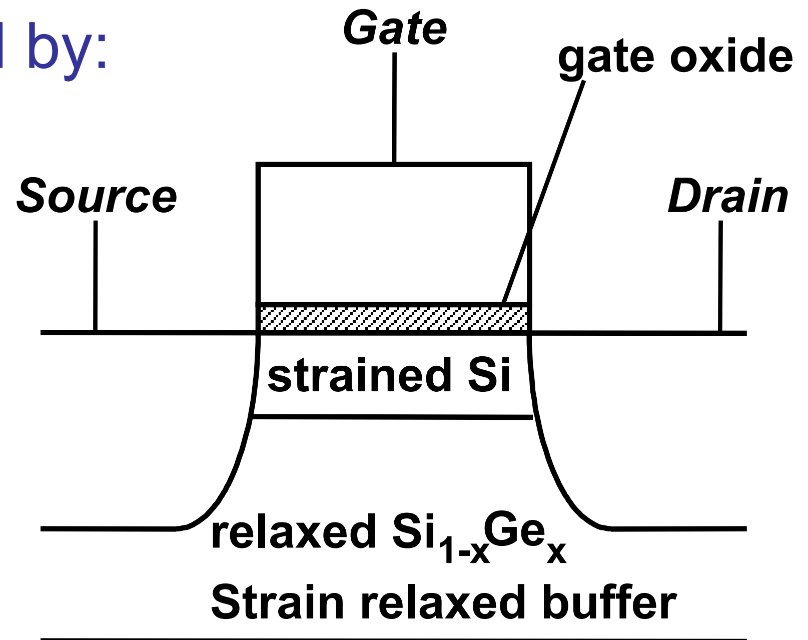
thin substrate


1000
100
10
1
Critical thickness (nm)
0
0.2
0.4
0.6
0.8
1
Ge fraction x (Si 1-x Ge x)
relaxed with dislocations
Si0.82Ge0.18
80 nm
30 nm
metastable
12 nm
stable

Which Device Characterization?

Device Performance improved by:

- high on current
  - Strain, surface roughness, defects, self heating
- low off current
  - Defects, doping



→ AFM, Optical Surface Profilometry, Defect Etch, Raman, AC Conductance

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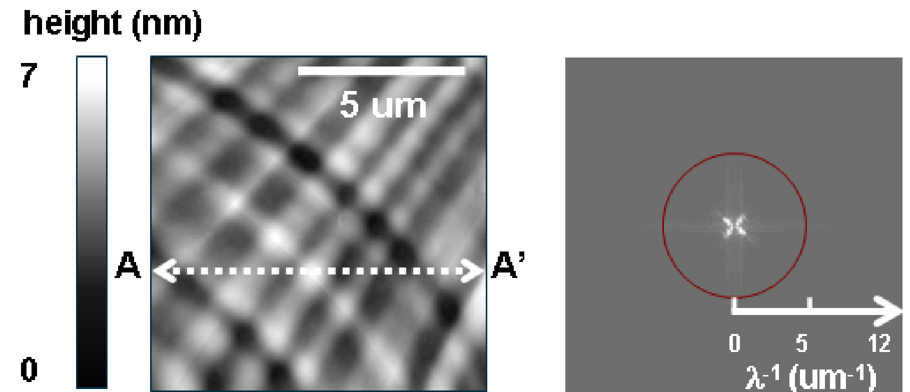
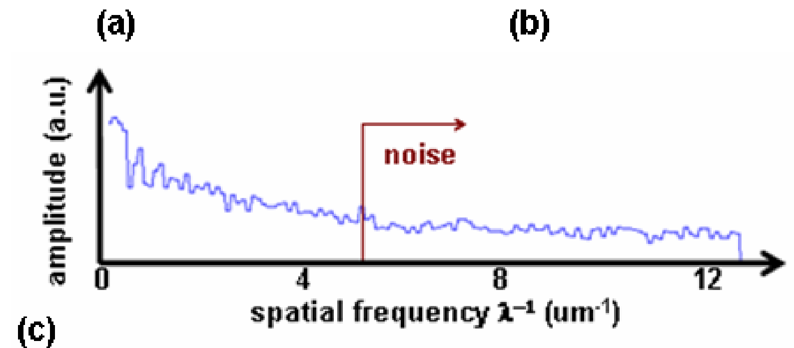
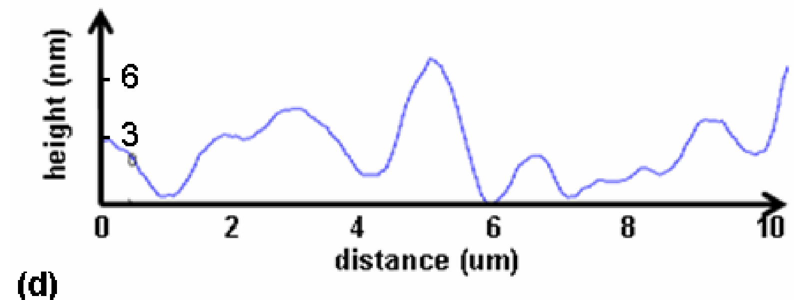
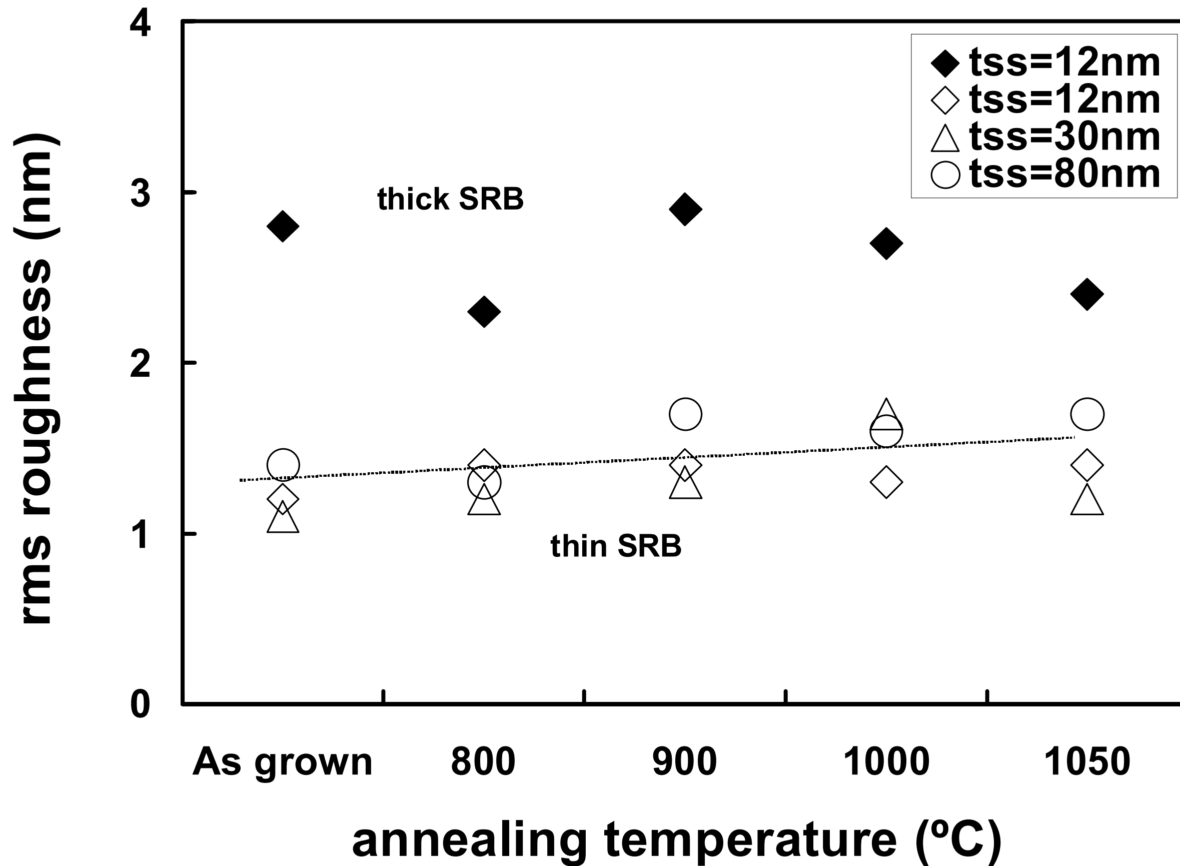
AFM

- 12nm SSi, annealed at 1000C for 30 s in N_2 (inert ambient)
- 256 points/s, area 10x10 μm^2
- 3 sites/sample (median given)
- Filter everything below 200 nm (noise), i.e. spatial frequency range: $12.8 > \lambda^{-1} > 5$ μm^{-1}
- Outside circle is filtered noise
- Peak-peak variation ~ 6 nm



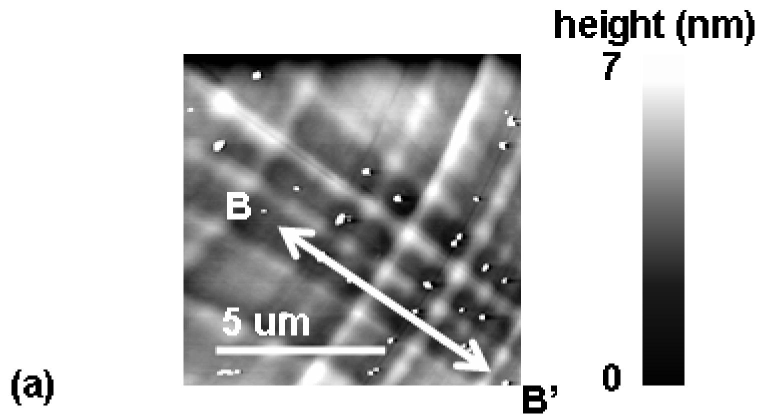


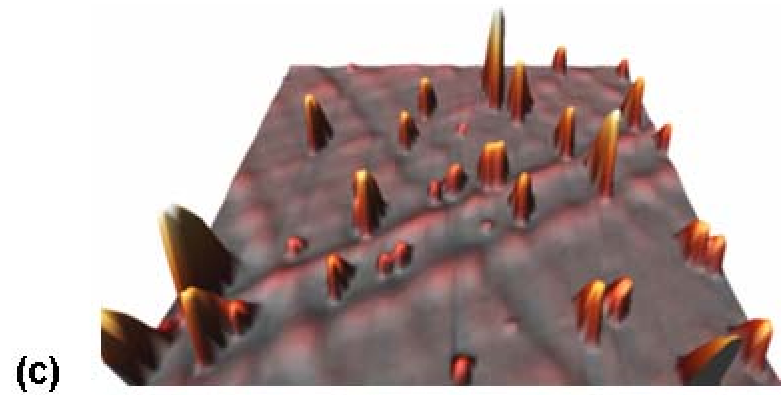


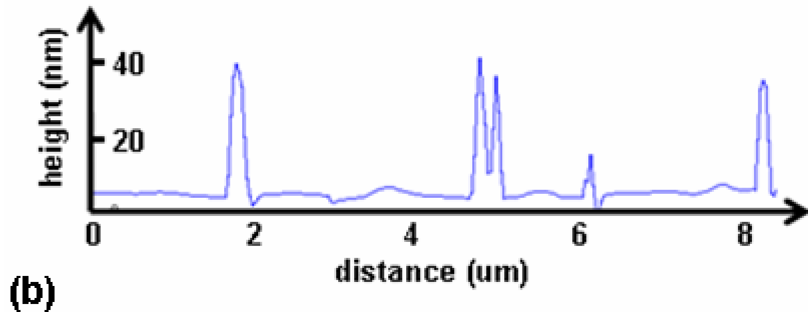


- Thin SRB has reduced roughness by ~50% compared with thick.
- Annealing has minor impact
- SSi thickness does not affect median surface roughness
- Trends confirmed by optical surface profiler

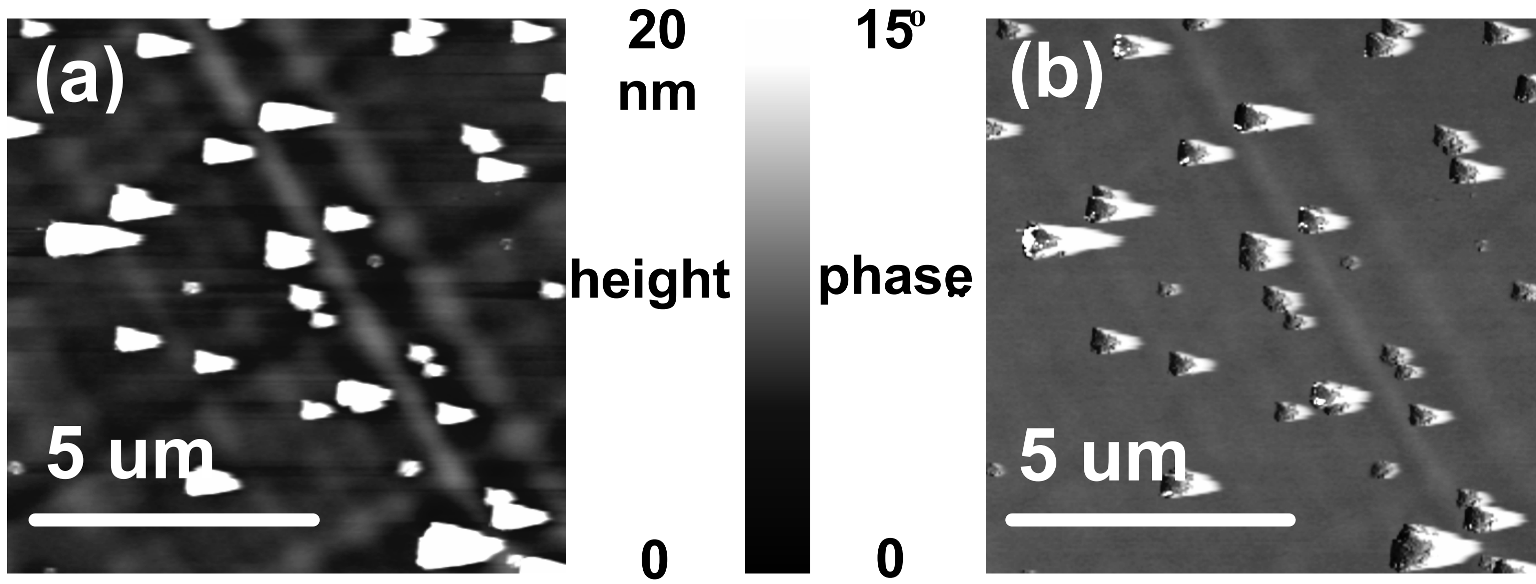
Closer inspection of AFM data revealed major differences due to t_{SSi}…







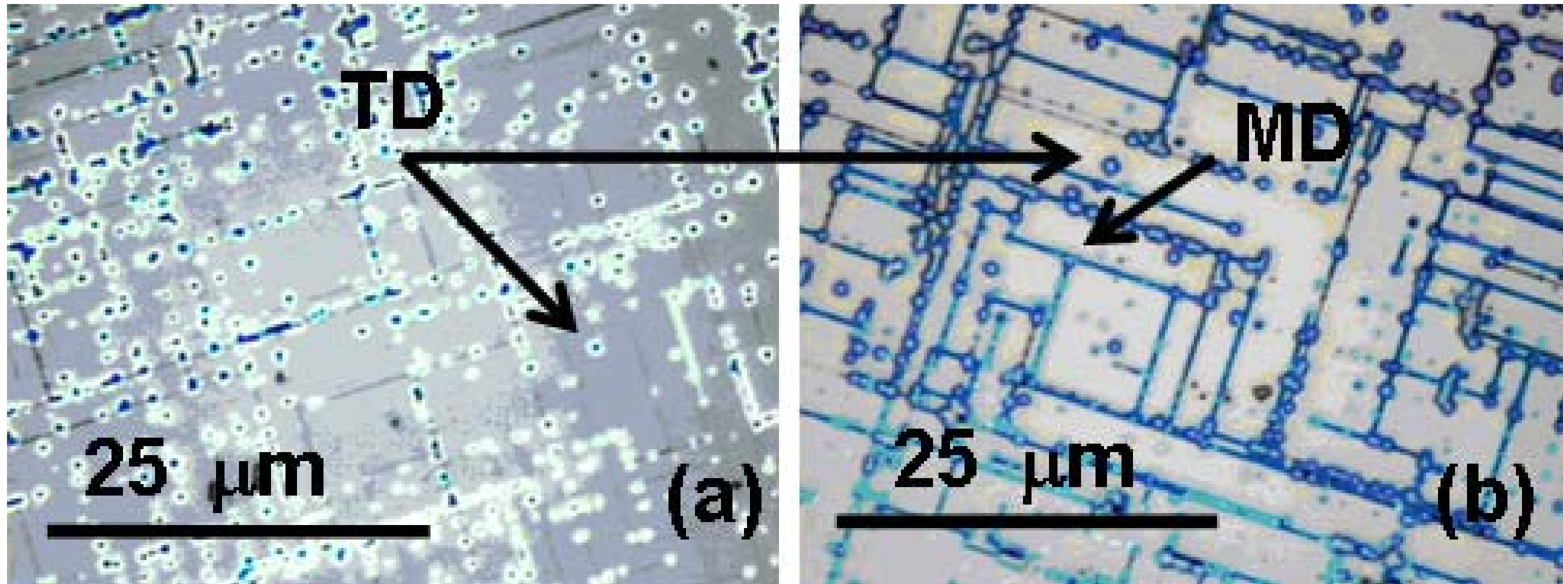
- 30 nm and 80 nm samples exhibit defects which protrude ~40 nm
- Surface defect density increases with annealing temperature and with SSi thickness
- 12 nm samples are defect free following all anneals
- Defects align with cross-hatching, occupying deepest valleys



- Phase mode AFM used to determine if defects are due to external contaminents.
- Small phase change detected → defect must be Si or SiO_2

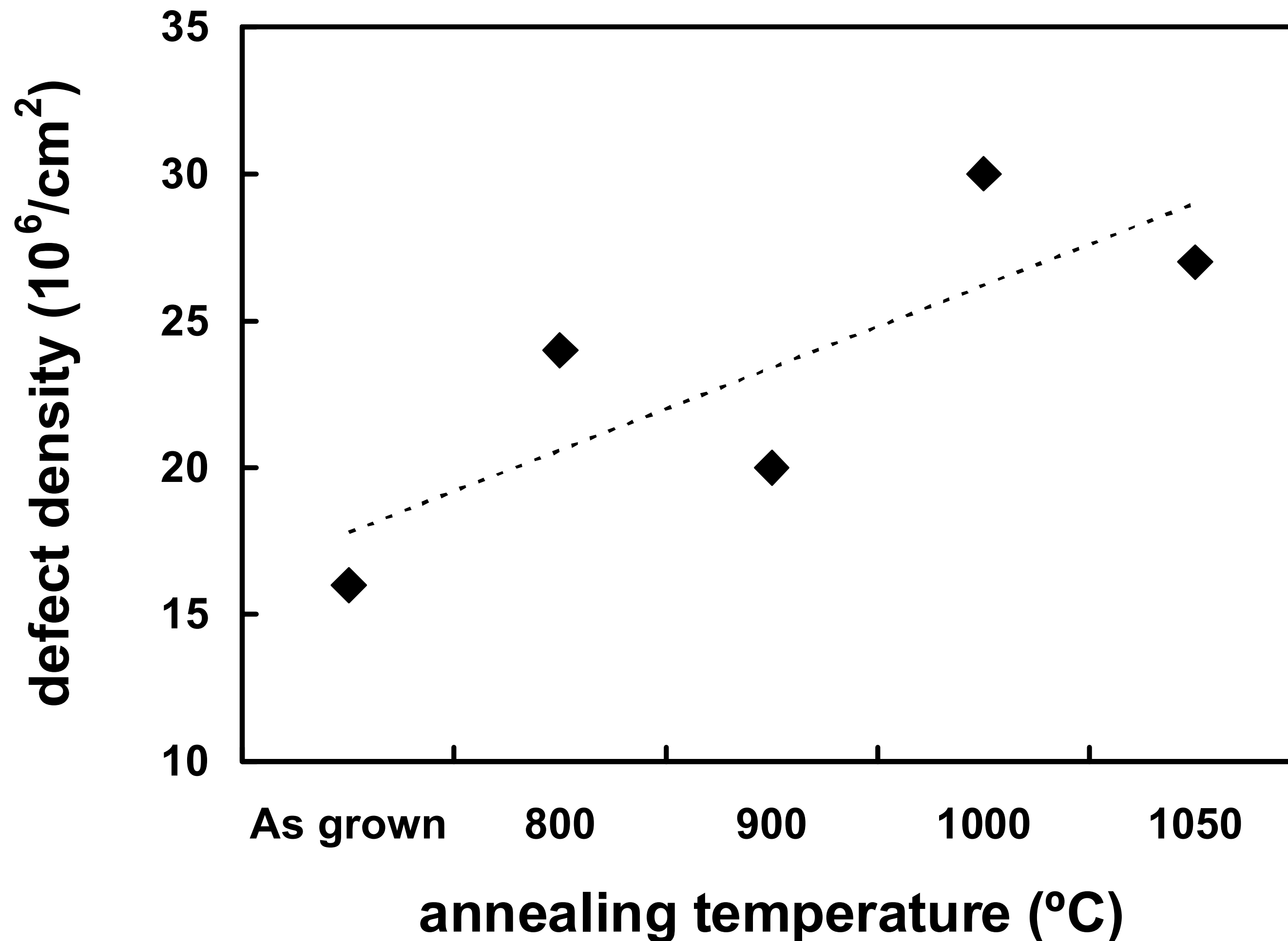
Defects are not observed with optical profiler

Defect Etching



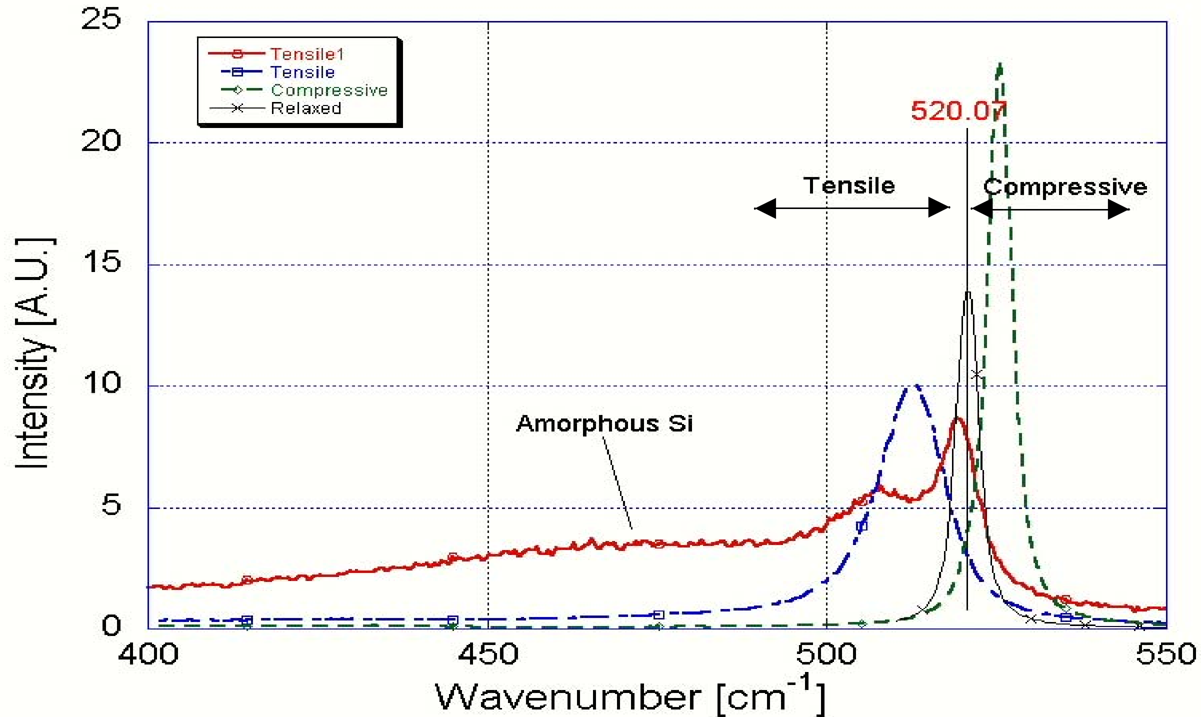
As-grown | Following 1000C anneal

- Defect etch used to reveal dislocations
- Before annealing only Threading Dislocations (TD) visible
- After annealing also see Misfit Dislocations (MD)
- Surface defects seen by AFM are linked to misfit dislocations (+ correlation with cross-hatch pattern).
- Height of defects indicates they are not themselves dislocations

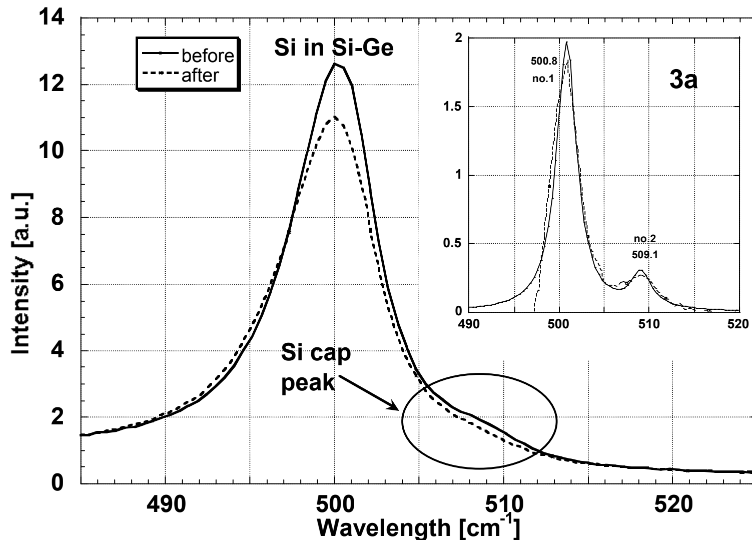


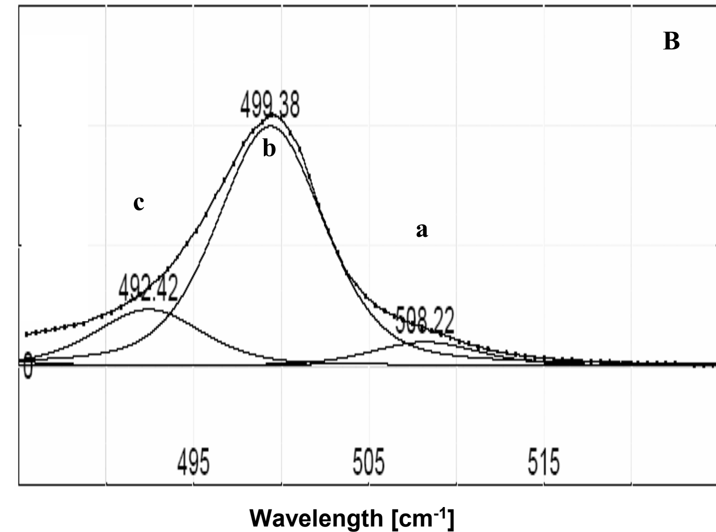
- Increased defect density as anneal temperature rises (80 nm data)
- Annealing → further strain relaxation
- Localized threading dislocations at ends of misfit dislocations reach SSi/SRB interface and seed stacking faults in SSi → surface defects

Raman Spectroscopy



- Used to study vibrational, rotational, and other low-frequency modes in various oscillating systems (e.g. molecules, crystals).
- It relies on inelastic scattering of monochromatic light
- photon energy is shifted up or down.
  $\rightarrow$ phonon modes in the system.
  $\rightarrow$ composition, structure, orientation, state (T, stress,etc.)
- Measure light intensity versus Raman shift
  - measured as $(\text{wavelength})^{-1}$

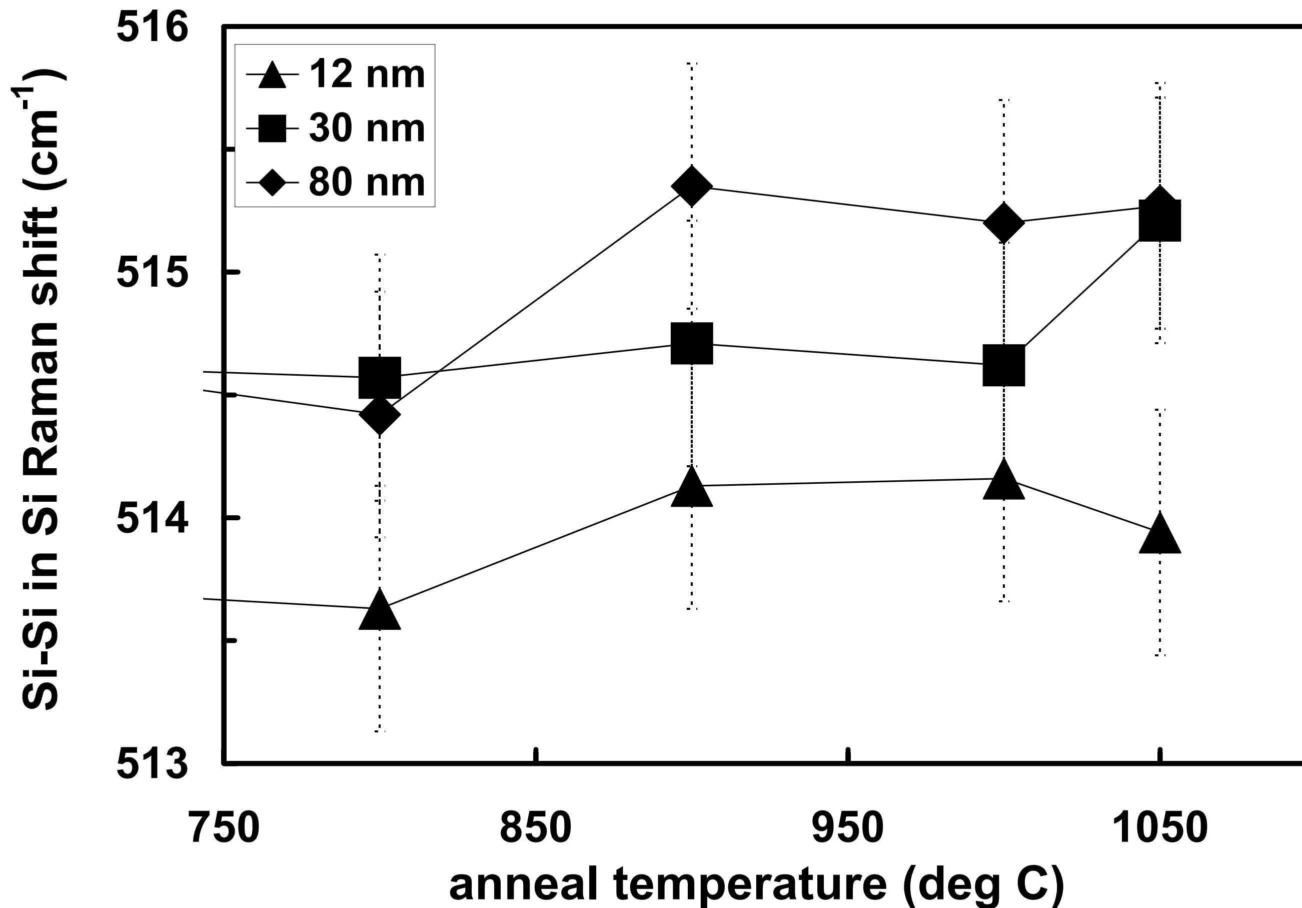




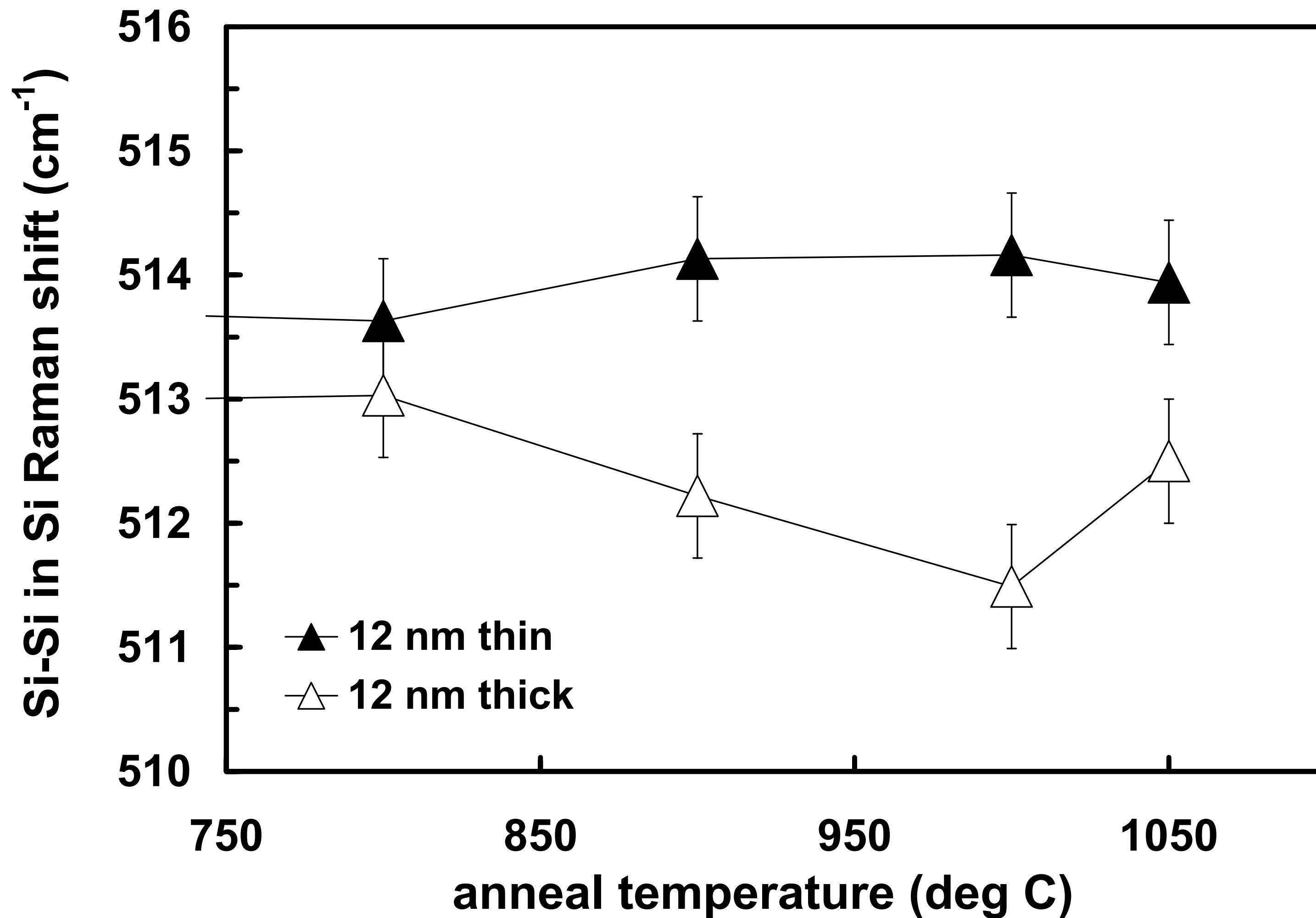
Measure, etch, measure, subtract, fit (double Lorenzian)

Measure, fit (PEAKFIT software)

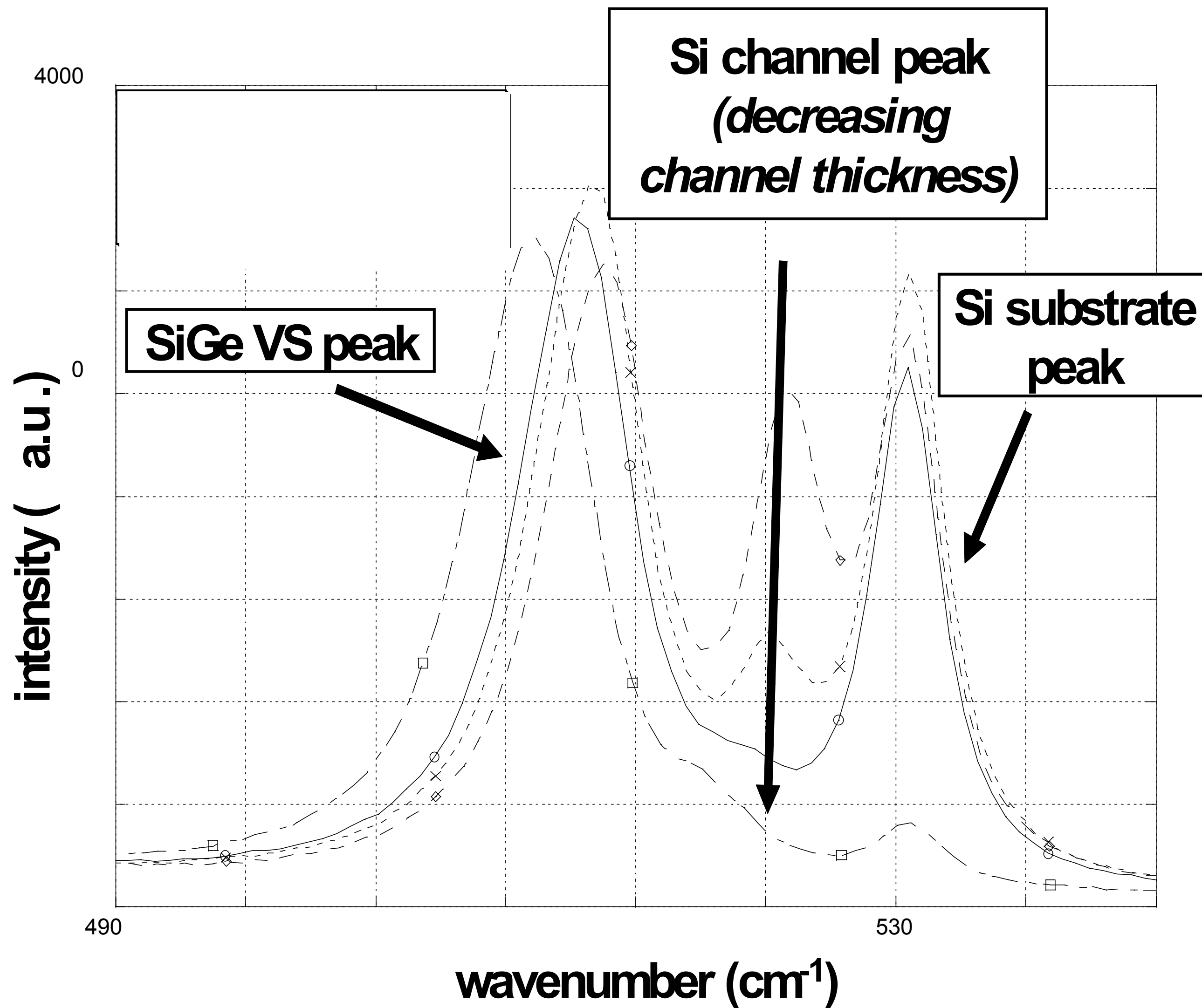
- Weak peak due to Si-Si in Strained Si is partially hidden by Si-Si peak from SiGe SRB.
- Use peak-fitting procedure calibrated against samples where selective etch removes SSi
- Good agreement between results
- Peak-fitting preferred (non-destructive)



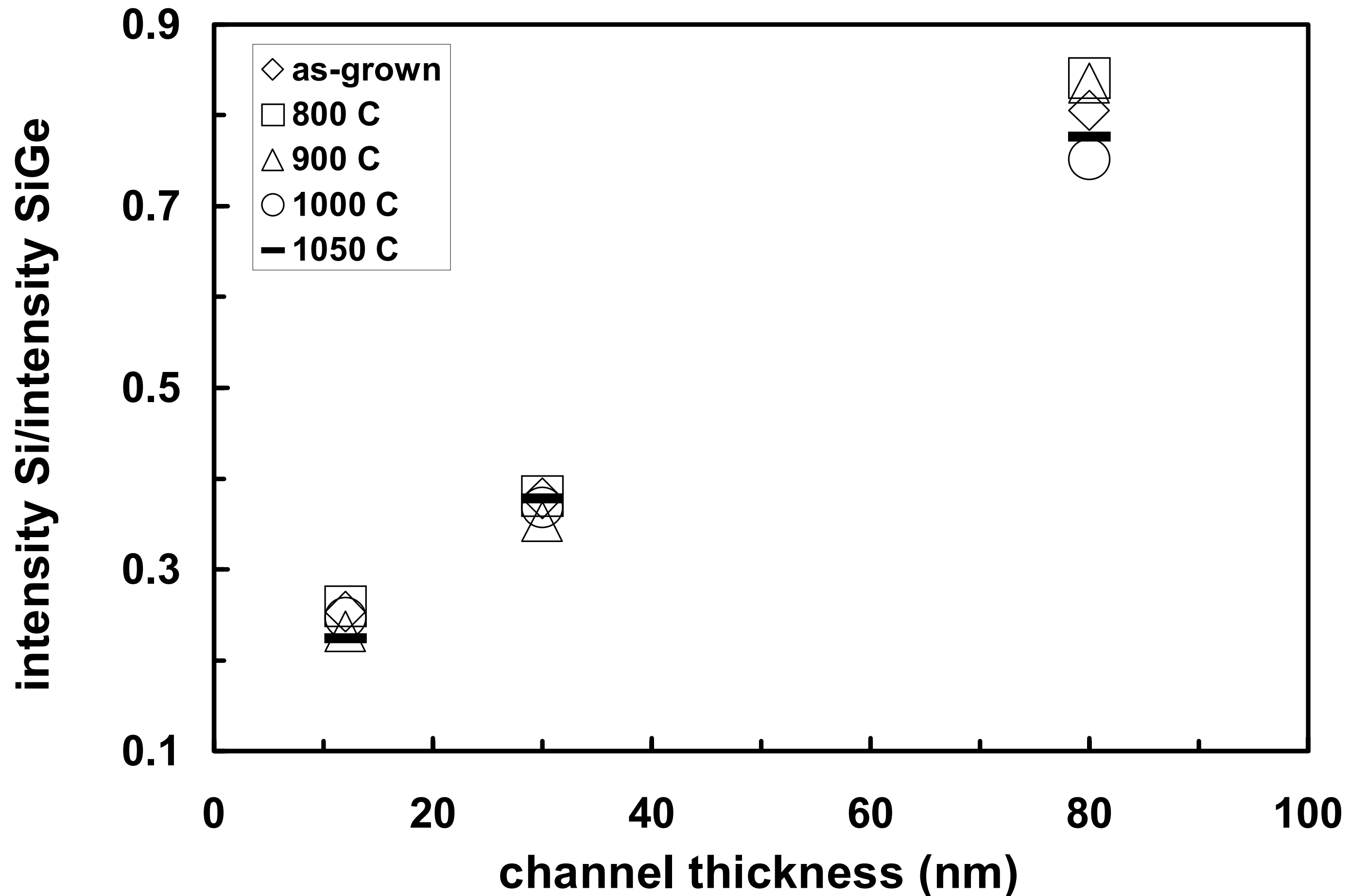
- Comparing strain in samples with 12, 30, 80 nm SSi layer
- In 12 nm sample strain is largest and no sign of relaxation with anneal
- In 30 nm sample there is distinct increase in relaxation at 1050C
- In 80 nm sample there is distinct increase in relaxation at 900C



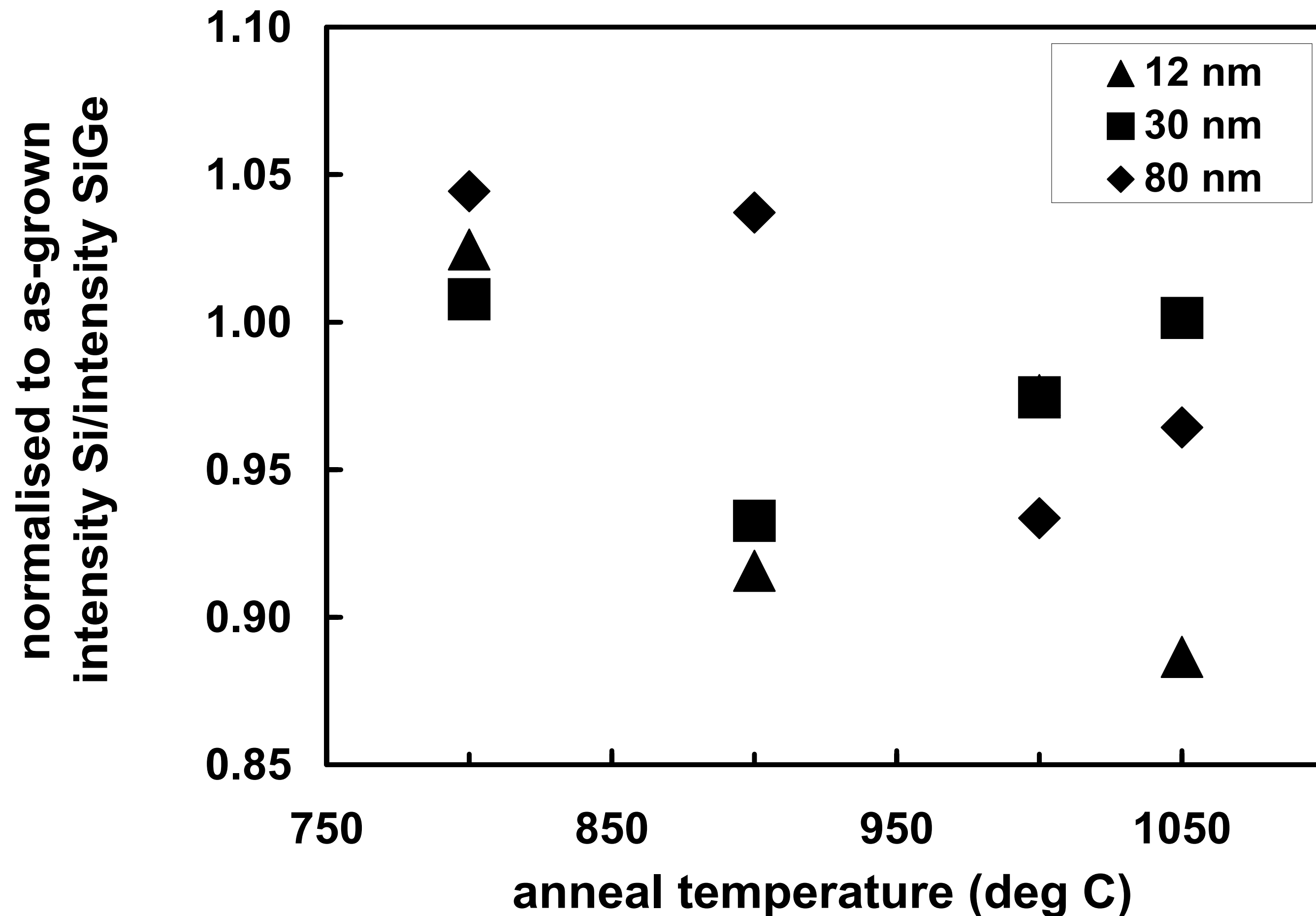
- Comparison between thin and thick SRB having 12 nm SSi.
- Thick SRB is lower so is providing (slightly) greater strain



- Intensity of Si-Si signal from SSi can indicate SSi thickness
- Thickness of SRB is same for each sample

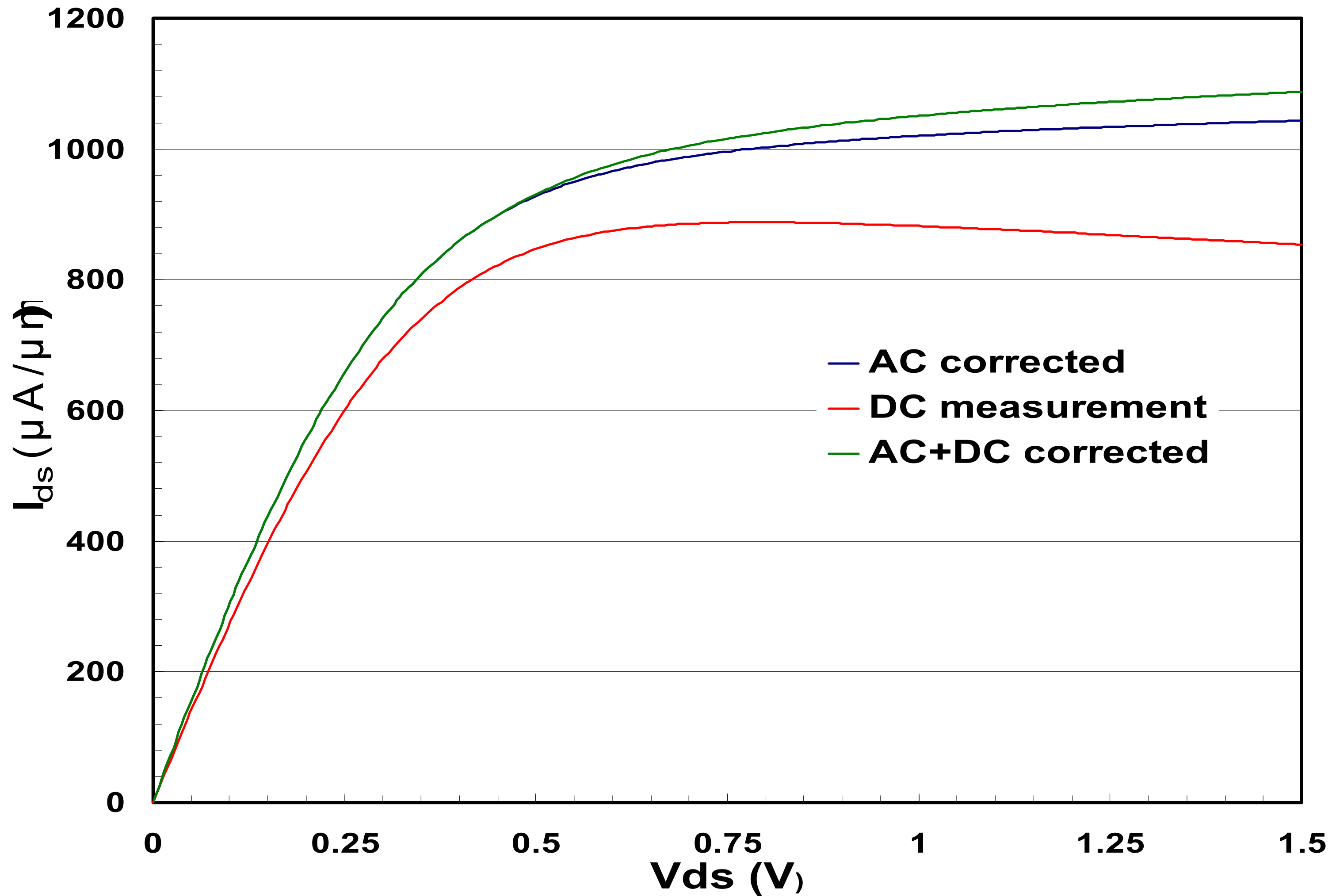


- Plot of relative intensity of Si/SRB correlates with channel thickness
- Can we use this method to measure Ge out-diffusion through SSi?

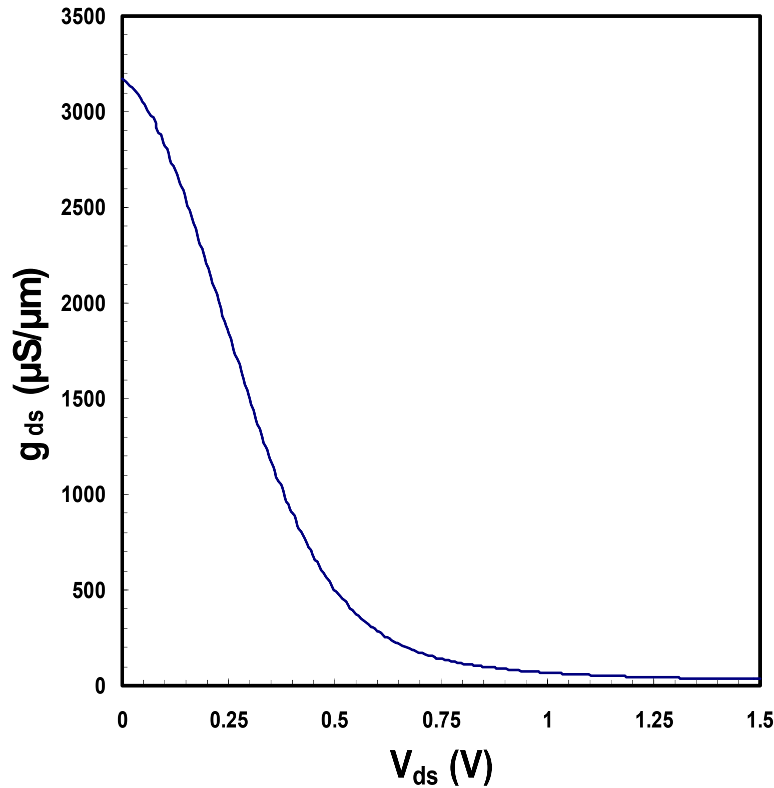


- TCAD predicts a Ge diffusion $\sqrt{Dt}$ ~ 2 nm
- Trends are not clear, but....
- See largest drop in intensity with 12 nm sample (as expected)

AC Conductance



AC Conductance



- Measure g_{ds} versus V_{ds} at high frequency
- Integrate:
  - $\int g_{ds}\, dV_{ds} = I_d$

  to recover I_d with ac self-heating removed

- Requires further correction to remove dc component

AC Conductance

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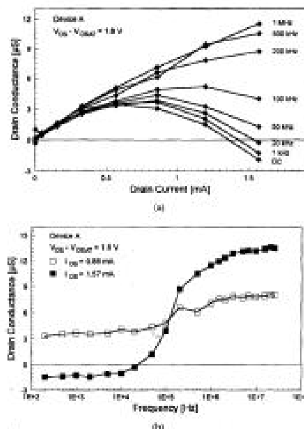

Fig. 2. Small signal drain conductance in saturation measured on a 20/5 µm partially depleted SIMOX NMOSFET (device A in Table I) with body tied to source, plotted versus (a) drain bias current and (b) versus frequency.

outlined in Section III. The saturation drain current model used here is based on (1), with an additional term to represent channel length modulation

$$I_{DS}=I_{Dsat}\,(1+\lambda V_{DS}) \qquad (5)$$

where λ is the channel length modulation factor and I_{Dsat} is the drain current from (1), evaluated at the drain saturation voltage ($V_{DS}=V_{Dsat}$). Although this is a relatively simple drain current model, it will be shown to be sufficiently accurate for the electro-thermal analysis demonstrated here. For accurate characterization of deep-submicron devices, a more complex model may be required as a starting point but an essentially identical derivation can be followed, which will, however, be more complex.

Combining (1) to (5) gives an expression for the drain current in saturation including self-heating effects shown in (6) at the bottom of the page.

In this expression $\beta_0=\mu_{eff,0}C_{ox}W/L$ is the transconductance parameter at the ambient temperature T_0. To simplify further analysis, three temperature dependent terms can be identified in (6), denoted by X, Y, and Z as indicated.

Differentiating (6) with respect to the drain voltage V_{DS} to obtain an expression for the drain conductance g_{DS} gives

$$g_{DS}=\frac{dI_{DS}}{dV_{DS}}=\frac{\partial I_{DS}}{\partial V_{DS}}+\frac{\partial I_{DS}}{\partial T}\frac{dT}{dV_{DS}}. \qquad (7)$$

Since V_{Dsat} does not depend on V_{DS}, the first term on the right hand side of (7) can be written as

$$\frac{\partial I_{DS}}{\partial V_{DS}}=\frac{\partial X}{\partial V_{DS}}\frac{Y}{Z}. \qquad (8)$$

This term can be identified as the drain conductance at a constant elevated temperature T, without the influence of *dynamic* self-heating effects. This is the conductance level measured at high frequencies (see Fig. 2) and will be denoted by g_{DST}.

Note that $\partial I_{DS}/\partial V_{DS}\equiv g_{DST}$ is not the drain conductance without self-heating, but merely the drain conductance at a *constant* temperature, significantly higher than ambient due to the power dissipated by the static bias current applied during the small signal measurement. The saturated drain conductance without self-heating effects, g_{DS0}, is defined as

$$g_{DS0}=\left.\frac{\partial I_{DS}}{\partial V_{DS}}\right|_{T=T_0}.$$

The difference between g_{DST} and g_{DS0} becomes very clear when (8) is rewritten as

$$g_{DST}=\frac{g_{DS0}\left(1+\dfrac{V_{Dsat}}{LE_{sat0}}\right)+\beta_0\chi(T-T_0)V_{Dsat}\lambda}{\left(1+\dfrac{V_{Dsat}}{LE_{sat}}\right)\cdot\left(\dfrac{T}{T_0}\right)^{-k}}$$

where E_{sat0} denotes the critical field at the ambient temperature T_0. Note that integration of g_{DST} does not simply give the drain current without self-heating as has been suggested by others [11]. The difference is significant even for small temperature rises.

The second term on the right hand side of (7) can be solved as

$$\frac{\partial I_{DS}}{\partial T}=\frac{\partial X}{\partial T}\frac{Y}{Z}+\frac{X}{Z^2}\left(Z\frac{\partial Y}{\partial T}-Y\frac{\partial Z}{\partial T}\right) \qquad (9)$$

$$I_{DS}=\overbrace{\beta_0(V_{GS}-V_{T0}+\chi(T-T_0)-\tfrac{1}{2}V_{Dsat})V_{Dsat}(1+\lambda V_{DS})}^{X}\,\frac{\overbrace{\left(\dfrac{T}{T_0}\right)^{-k}}^{Y}}{\underbrace{\left(1+\dfrac{V_{Dsat}}{LE_{sat}}\right)}_{Z}} \qquad (6)$$

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where the partial differentials can be further evaluated as:

$$\frac{\partial X}{\partial T}=\beta_0\,\chi\,V_{Dsat}(1+\lambda V_{DS}) \qquad (10)$$

$$\frac{\partial Y}{\partial T}=-\frac{k}{T}\left(\frac{T}{T_0}\right)^{-k} \qquad (11)$$

$$\frac{\partial Z}{\partial T}=-\frac{V_{Dsat}}{L\,E_{sat}^2}\frac{d}{dT}\left(\frac{2v_{sat}}{\mu_{eff}}\right)=-\frac{V_{Dsat}}{L\,E_{sat}}\left\{\frac{k}{T}-\frac{0.8\exp\left(\dfrac{T}{600}\right)}{600\left[1+0.8\exp\left(\dfrac{T}{600}\right)\right]}\right\}. \qquad (12)$$

The local device temperature T can be expressed in terms of the power dissipation $I_{DS}V_{DS}$ and the total thermal resistance from the device to ambient R_T as:

$$T=T_0+R_TV_{DS}I_{DS}. \qquad (13)$$

Using this expression, the last term in (7) can be solved as

$$\frac{dT}{dV_{DS}}=\frac{\partial T}{\partial V_{DS}}+\frac{\partial T}{\partial I_{DS}}\frac{dI_{DS}}{dV_{DS}}=R_T\,I_{DS}+R_T\,V_{DS}\,g_{DS}=(T-T_0)\left(\frac{1}{V_{DS}}+\frac{g_{DS}}{I_{DS}}\right). \qquad (14)$$

Combining (7) to (14) gives a general expression for the small signal drain conductance in saturation, including static and dynamic self-heating effects shown in (15) at the bottom of the page.

Since I_{DS}, V_{DS}, V_{Dsat}, g_{DS}, g_{DST}, and T_0 are all directly measurable variables, this equation can be used effectively to extract the only unknown variable, the local device temperature T. Equation (15) cannot be written explicitly in terms of T due to the nonlinear temperature dependence of E_{sat}, but can be solved accurately using standard numerical techniques. When the local device temperature T is known, the total thermal resistance R_T can easily be calculated from (13).

The expression for the temperature dependent drain conductance in saturation derived thus far has a wide applicability, but its accuracy is not always required. When measurements are made at high static gate biases, the influence of the temperature dependence of the threshold voltage will be small (i.e., when $\chi\,\Delta T\ll V_{GS}$). Furthermore, the influence of carrier velocity saturation will only be significant for short channel devices. Hence, for long channel devices with sufficiently high gate biases, the self-heating effect will be dominated by the temperature dependence of mobility. Following an identical analysis as before, but including only the temperature dependence of mobility (i.e., $\chi=0$ and $E_{sat}=\infty$), the expressions for drain conductance in saturation can now be solved analytically to yield an estimate of the temperature rise

$$T=T_0\left[1+\frac{g_{DST}-g_{DS}}{k\left(g_{DS}+\dfrac{I_{DS}}{V_{DS}}\right)-(g_{DST}-g_{DS})}\right]. \qquad (16)$$

V. Experimental Technique

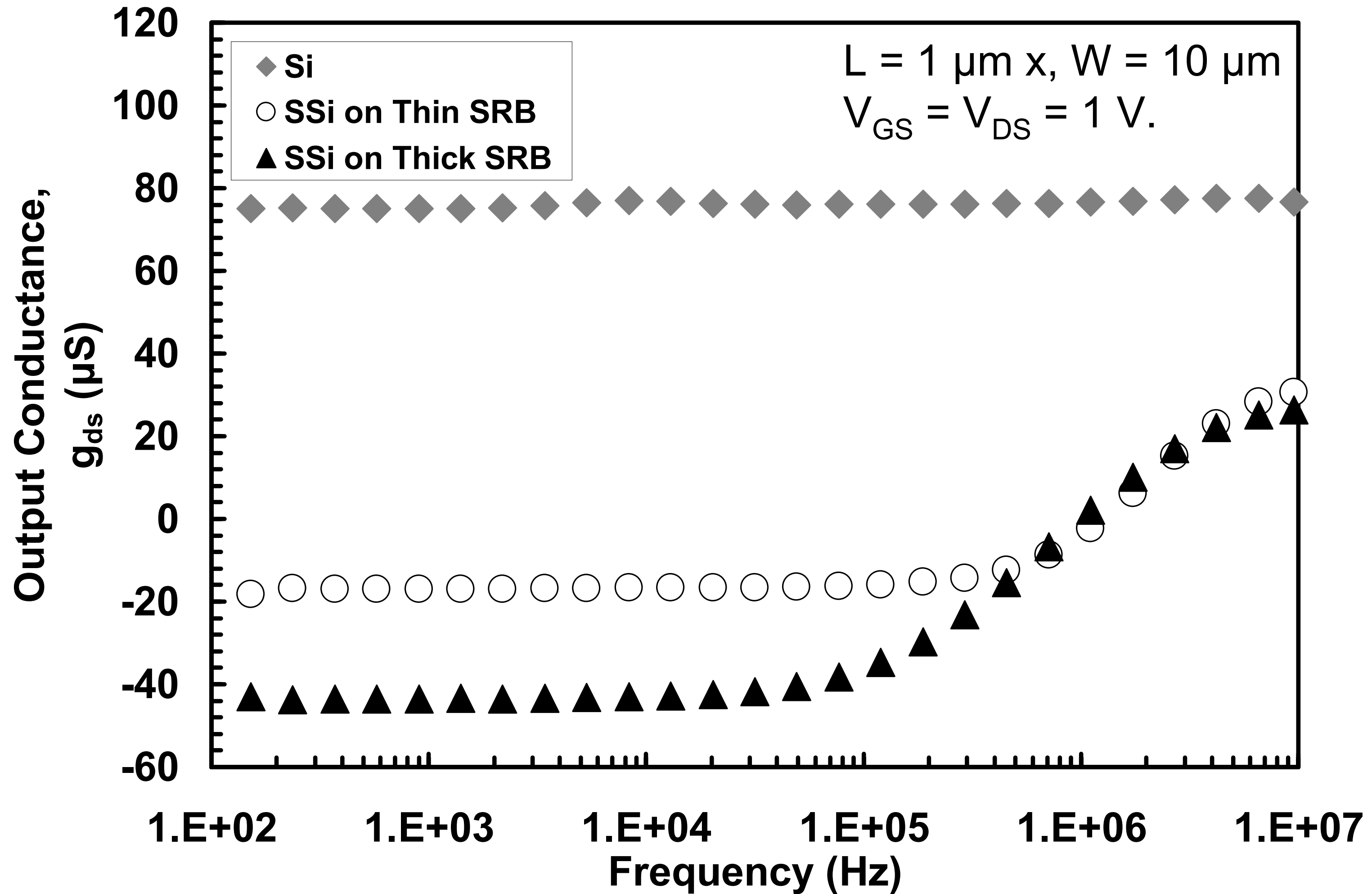
A. Conductance Measurements

To extract the total thermal resistance the small-signal drain conductance in saturation is measured as a function of frequency to determine the asymptotic LF and HF levels g_{DS} and g_{DST} as described in Section IV. The frequency range must extend sufficiently below the largest and above the smallest relevant thermal time-constant in the device. With thermal time-constants typically in the µs or ns range, conductance must be measured over a wide frequency range, usually exceeding the capability of a single instrument.

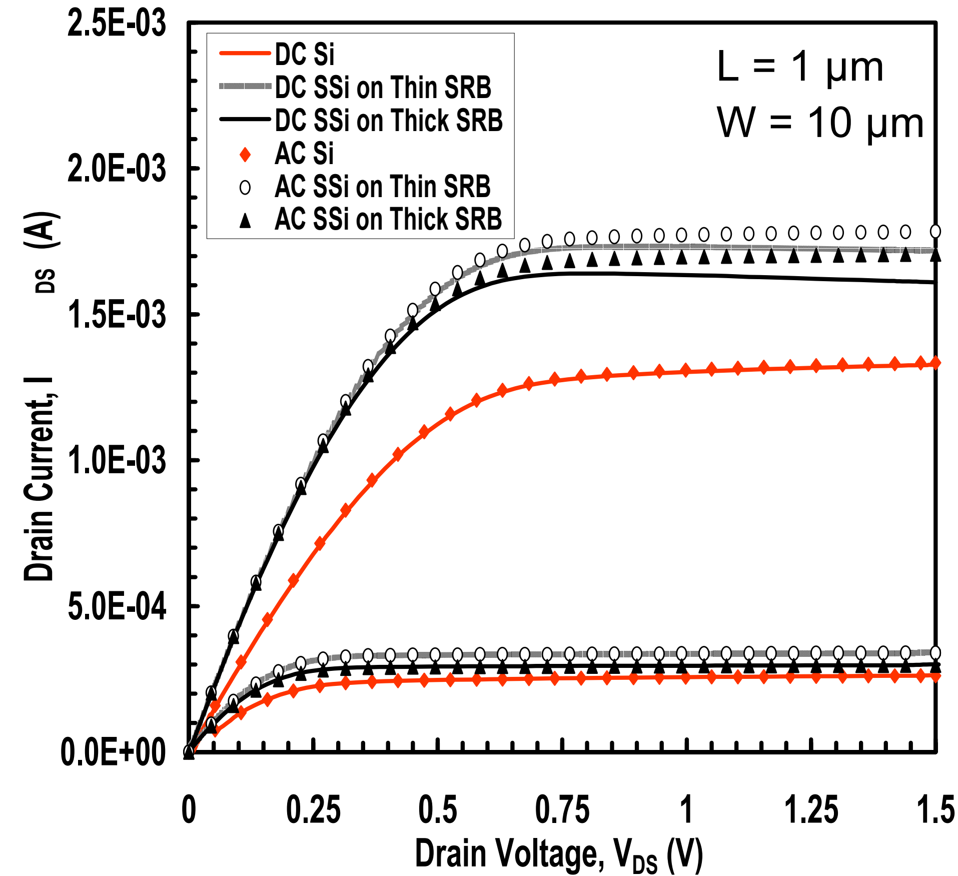
In this study, a combination of the HP 4192A and HP 4291A LF and RF Impedance Analyzers has been used to cover the frequency range of 5 Hz–1.8 GHz. In addition, an HP 4155A Parameter Analyzer has been used for static measurements of bias voltages and currents. Although several analyzers and, hence, several measurement techniques are used, all measurements must be made on the same device to obtain meaningful results. The ambient temperature during all measurements must be carefully controlled to ensure consistency of results. Both the low and high frequency parts of the measurement have particular complications.

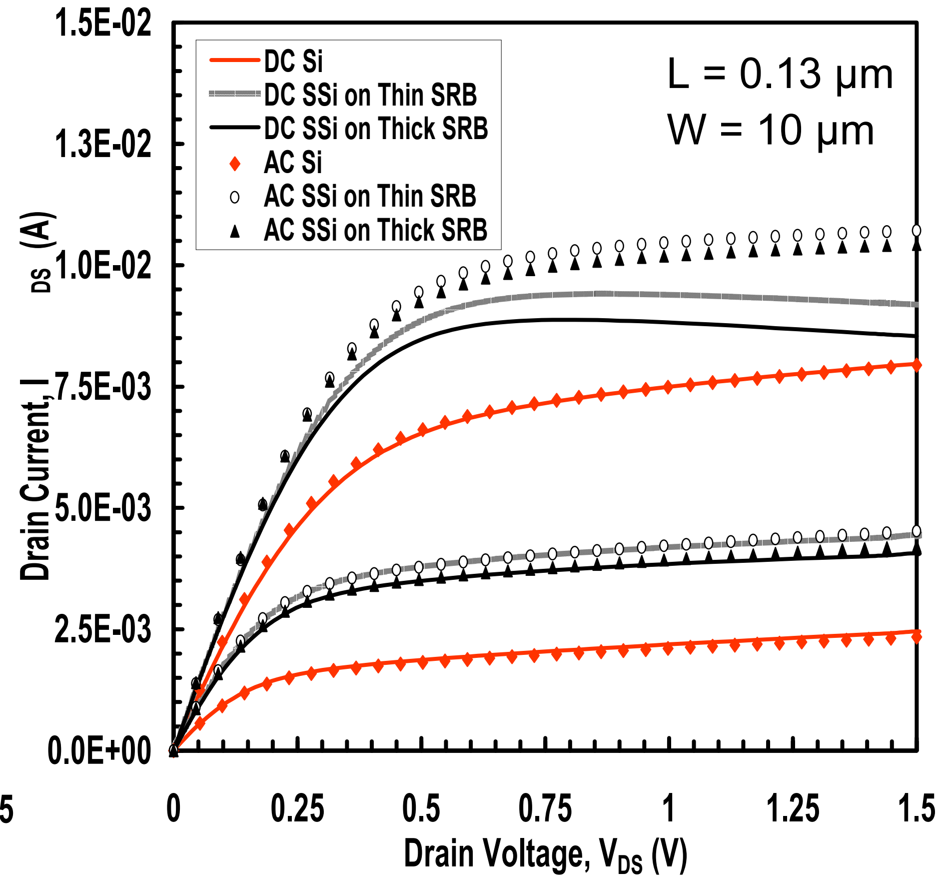
Fig. 3 shows the setup used for the low frequency conductance measurements. A major problem here is the large series resistance (up to a few kΩ) in the internal bias circuit of the HP 4192A, causing a significant error in the static drain bias applied to the device under test even at moderate drain currents. This error is corrected by measuring the actual bias across the terminals of the test device with a digital volt meter and iteratively setting the correct bias on the HP 4192A. A CMOS instrumentation amplifier with very high input impedance is used to prevent any influence of

$$g_{DS}=g_{DST}+(T-T_0)\left(\frac{1}{V_{DS}}+\frac{g_{DS}}{I_{DS}}\right)\left[\frac{\beta_0\,\chi\,V_{Dsat}(1+\lambda V_{DS})\left(\dfrac{T}{T_0}\right)^{-k}}{\left(1+\dfrac{V_{Dsat}}{LE_{sat}}\right)}-\frac{k\,I_{DS}}{T}-\frac{I_{DS}\,V_{Dsat}}{L\,E_{sat}+V_{Dsat}}\left\{\frac{0.8\exp\left(\dfrac{T}{600}\right)}{600\left[1+0.8\exp\left(\dfrac{T}{600}\right)\right]}-\frac{k}{T}\right\}\right] \qquad (15)$$

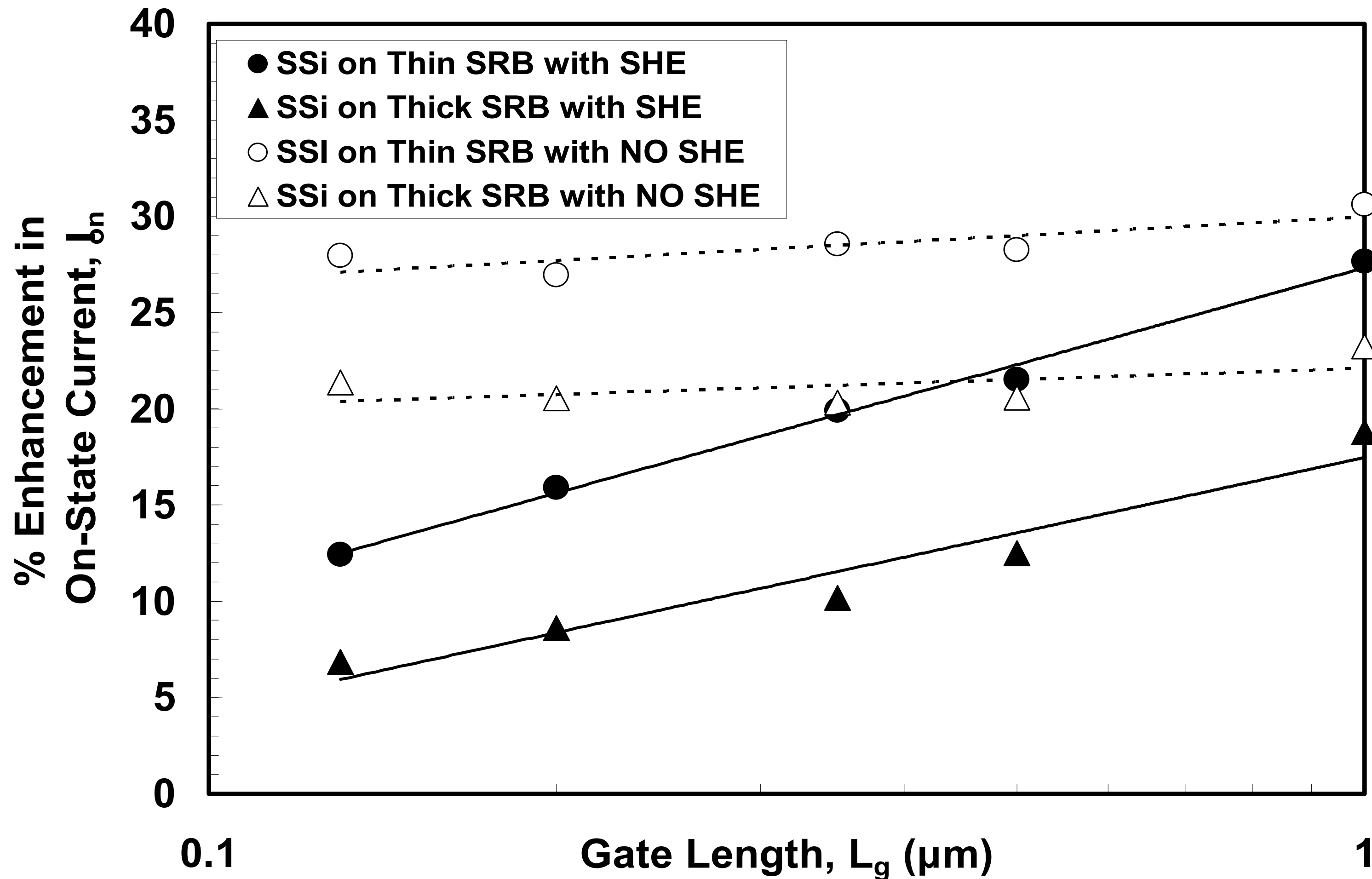


- Control Si data independent of frequency
- Gds goes from –ve to +ve for SSi devices
- Larger effect for thick SRB
- Both reach asymptotic level as dynamic self heating is suppressed





- Vgs = 0.05, 1V
- More self-heating at higher Vgs, thick SRB
- Thermal resistance is 10.56 $K.mW^{-1}$ (thin) and 18.54 $K.mW^{-1}$ (thick)



- Reduced enhancement in device performance as gate length scales for devices on SRBs is attributed to three major factors: self-heating, loss of strain, increased parasitics
- AC conductance shows that self-heating is the major factor reducing performance as L_g scales in these devices.

Outline

- Strained Silicon MOSFETs
- Thin Strain Relaxed Buffer (SRB) MOSFETs
- Characterization
- Summary

Summary

- AFM showed surface defects that are not visible to optical profiling.
- Combined with defect etching these defects are shown to correlate with misfit dislocations.
- Raman measurements show strain relaxation in supercritical SSi layers.
- AC conductance shows that self-heating is the major contribution to reduced performance as Lg reduces.

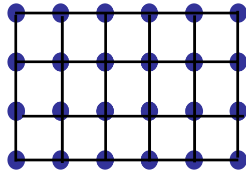
Acknowledgements

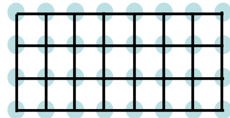
- EC Network of Excellence for Silicon in Nanoelectronics (SiNANO)
- UK Engineering and Physical Sciences Research Council (EPSRC)
- Atmel Corporation

Strained Si: Virtual Substrate

Global strain

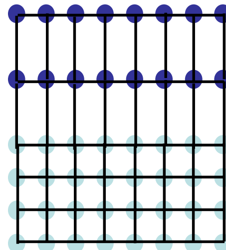
$Si_{0.75}Ge_{0.25}$
1 % expansion



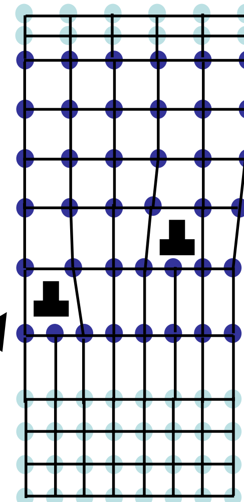


Si
a=5.43Å

Pseudomorphic SiGe layer coherently strained



Tensile strained Si layer on SiGe 'virtual substrate'



Above a critical thickness the SiGe layer relaxes strain with misfit dislocations

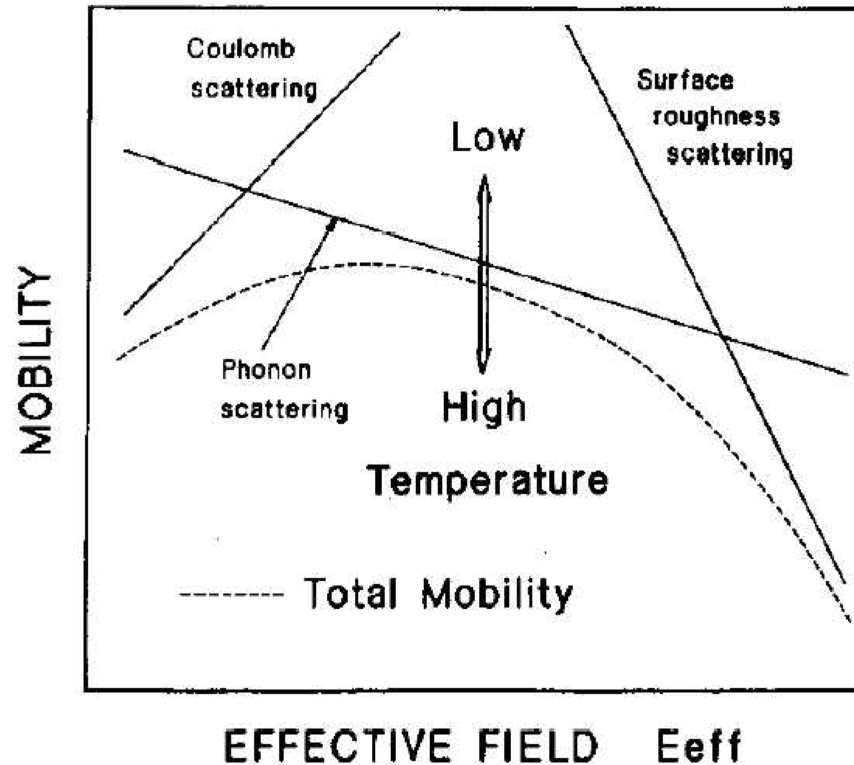
Thermal Resistance

$$Power = \kappa \frac{dT}{dx}$$

$$\Delta T = Power \times \frac{d}{\kappa}$$

$$V = I \times R$$

Mobility enhancements



- **Mobility dominated by different scattering mechanisms at different E_{eff}**
- **At room temperature:**
  - low E_{eff}: Coulomb, phonon
  - mid E_{eff}: phonon
  - high E_{eff}: surface roughness, phonon